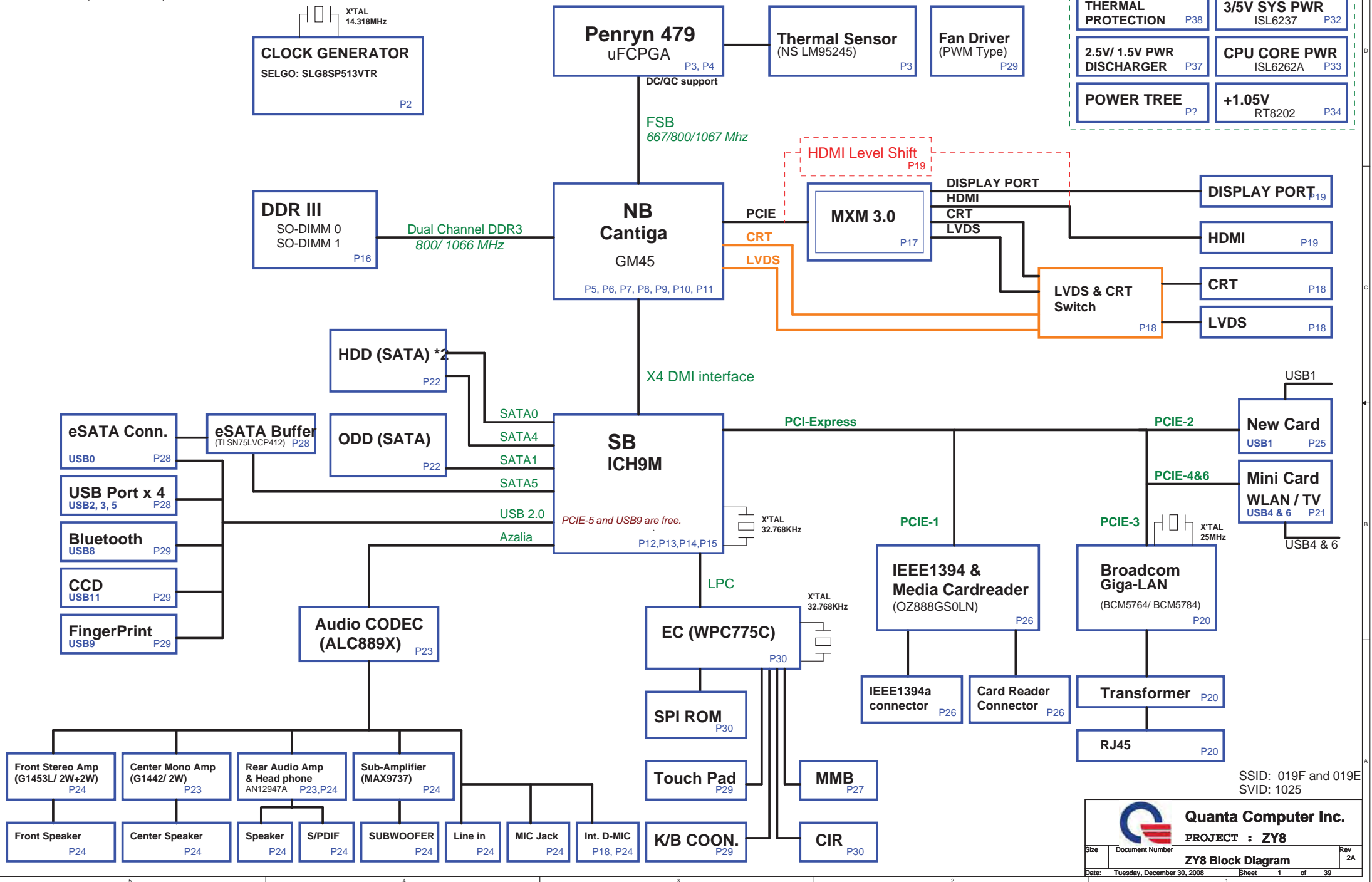
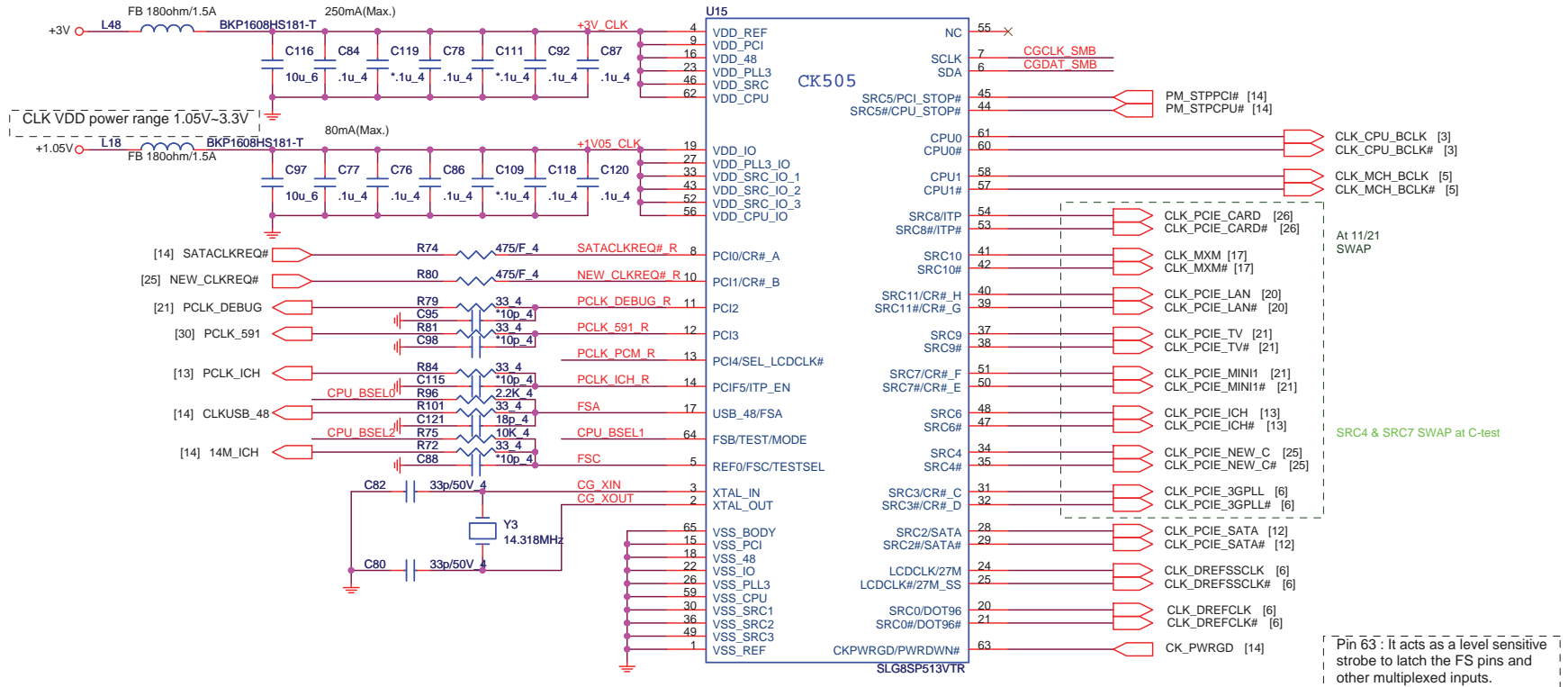


31ZY8MB0000  
ZY8 MB ASSY(DC/GM/MXM)ASSY W/O CPU  
31ZY8MB0010  
ZY8 MB ASSY(QC/GM/MXM)ASSY W/O CPU

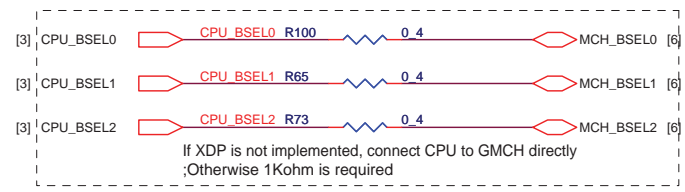
# ZY8 SYSTEM BLOCK DIAGRAM



Clock Generator



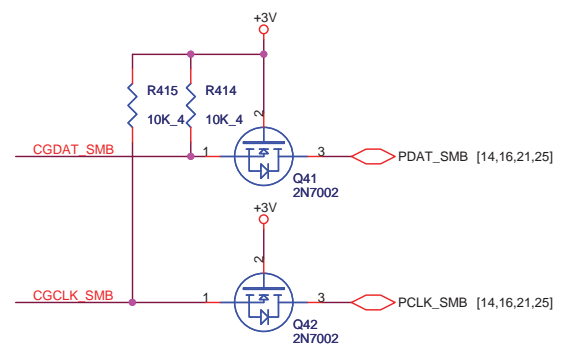
CPU Clock select



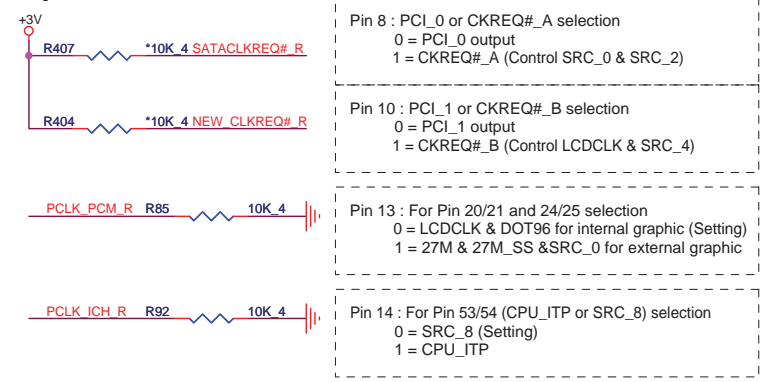
BSEL Frequency Select Table


FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

SMBus



Strap table





**Quanta Computer Inc.**  
PROJECT : ZY8

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**CLOCK GENERATOR**

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Rev 2A





	QCI P/N
Intel Cantiga (G)M	AJ0QV080T06

[3] H\_D# [0..63]

H\_D#0 F2  
H\_D#1 G8  
H\_D#2 F8  
H\_D#3 E6  
H\_D#4 G2  
H\_D#5 H6  
H\_D#6 H2  
H\_D#7 F6  
H\_D#8 D4  
H\_D#9 H3  
H\_D#10 M9  
H\_D#11 M11  
H\_D#12 J1  
H\_D#13 J2  
H\_D#14 N12  
H\_D#15 J6  
H\_D#16 P2  
H\_D#17 L2  
H\_D#18 R2  
H\_D#19 N9  
H\_D#20 L6  
H\_D#21 M5  
H\_D#22 J3  
H\_D#23 N2  
H\_D#24 R1  
H\_D#25 N5  
H\_D#26 N6  
H\_D#27 P13  
H\_D#28 N8  
H\_D#29 L7  
H\_D#30 N10  
H\_D#31 M3  
H\_D#32 Y3  
H\_D#33 AD14  
H\_D#34 Y6  
H\_D#35 Y10  
H\_D#36 Y12  
H\_D#37 Y14  
H\_D#38 Y7  
H\_D#39 W2  
H\_D#40 AA8  
H\_D#41 Y9  
H\_D#42 AA13  
H\_D#43 AA9  
H\_D#44 AA11  
H\_D#45 AD11  
H\_D#46 AD10  
H\_D#47 AD13  
H\_D#48 AE12  
H\_D#49 AE9  
H\_D#50 AA2  
H\_D#51 AD8  
H\_D#52 AA3  
H\_D#53 AD3  
H\_D#54 AD7  
H\_D#55 AE14  
H\_D#56 AF3  
H\_D#57 AC1  
H\_D#58 AE3  
H\_D#59 AC3  
H\_D#60 AE11  
H\_D#61 AE8  
H\_D#62 AG2  
H\_D#63 AD6

U29A

H\_D#\_0  
H\_D#\_1  
H\_D#\_2  
H\_D#\_3  
H\_D#\_4  
H\_D#\_5  
H\_D#\_6  
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H\_A#\_34  
H\_A#\_35

A14 H\_A#3  
C15 H\_A#4  
F16 H\_A#5  
H13 H\_A#6  
C18 H\_A#7  
M16 H\_A#8  
J13 H\_A#9  
P16 H\_A#10  
R16 H\_A#11  
N17 H\_A#12  
M13 H\_A#13  
E17 H\_A#14  
P17 H\_A#15  
F17 H\_A#16  
G20 H\_A#17  
B19 H\_A#18  
J16 H\_A#19  
E20 H\_A#20  
H16 H\_A#21  
J20 H\_A#22  
L17 H\_A#23  
A17 H\_A#24  
B17 H\_A#25  
L16 H\_A#26  
C21 H\_A#27  
J17 H\_A#28  
H20 H\_A#29  
B18 H\_A#30  
K17 H\_A#31  
B20 H\_A#32  
F21 H\_A#33  
K21 H\_A#34  
L20 H\_A#35

H\_A# [3..35] [3]

H\_ADS# H12 H\_ADS# [3]  
H\_ADSTB#\_0 B16 H\_ADSTB#0 [3]  
H\_ADSTB#\_1 G17 H\_ADSTB#1 [3]  
H\_BNR# A9 H\_BNR# [3]  
H\_BPR# F11 H\_BPR# [3]  
H\_BREQ# G12 H\_BREQ# [3]  
H\_DEFER# E9 H\_DEFER# [3]  
H\_DBSY# B10 H\_DBSY# [3]  
HPLL\_CLK AH7 CLK\_MCH\_BCLK [2]  
HPLL\_CLK# AH6 CLK\_MCH\_BCLK# [2]  
H\_DPWR# J11 H\_DPWR# [3]  
H\_DRDY# F9 H\_DRDY# [3]  
H\_HIT# H9 H\_HIT# [3]  
H\_HITM# E12 H\_HITM# [3]  
H\_LOCK# H11 H\_LOCK# [3]  
H\_TRDY# C9 H\_TRDY# [3]

H\_DINV#\_0 J8 H\_DINV#0 [3]  
H\_DINV#\_1 L3 H\_DINV#1 [3]  
H\_DINV#\_2 Y13 H\_DINV#2 [3]  
H\_DINV#\_3 Y1 H\_DINV#3 [3]

H\_DSTBN#\_0 L10 H\_DSTBN#0 [3]  
H\_DSTBN#\_1 M7 H\_DSTBN#1 [3]  
H\_DSTBN#\_2 AA5 H\_DSTBN#2 [3]  
H\_DSTBN#\_3 AE6 H\_DSTBN#3 [3]

H\_DSTBP#\_0 L9 H\_DSTBP#0 [3]  
H\_DSTBP#\_1 M8 H\_DSTBP#1 [3]  
H\_DSTBP#\_2 AA6 H\_DSTBP#2 [3]  
H\_DSTBP#\_3 AE5 H\_DSTBP#3 [3]

H\_REQ#\_0 B15 H\_REQ#0 [3]  
H\_REQ#\_1 K13 H\_REQ#1 [3]  
H\_REQ#\_2 F13 H\_REQ#2 [3]  
H\_REQ#\_3 B13 H\_REQ#3 [3]  
H\_REQ#\_4 B14 H\_REQ#4 [3]

H\_RS#\_0 B6 H\_RS#0 [3]  
H\_RS#\_1 F12 H\_RS#1 [3]  
H\_RS#\_2 C8 H\_RS#2 [3]

H\_SWING C5  
H\_RCOMP E3

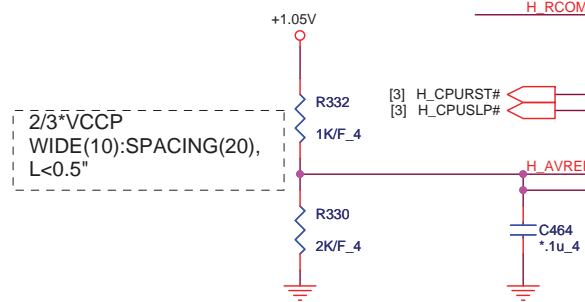
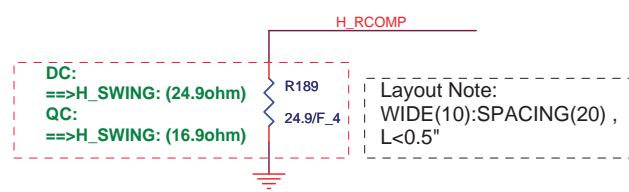
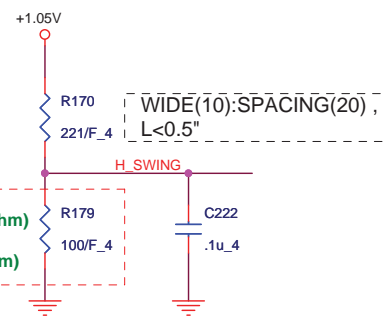
H\_SWING  
H\_RCOMP

[3] H\_CPURST# C12  
[3] H\_CPUSLP# E11

H\_CPURST#  
H\_CPUSLP#

H\_AVREF A11  
H\_DVREF B11

CANTIGA\_GM45



HOST



Quanta Computer Inc.

PROJECT : ZY8

GMCH HOST

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		3B

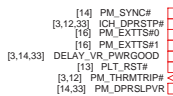
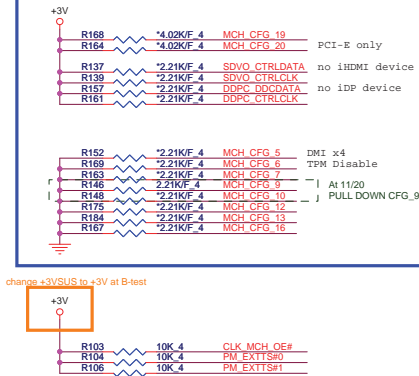
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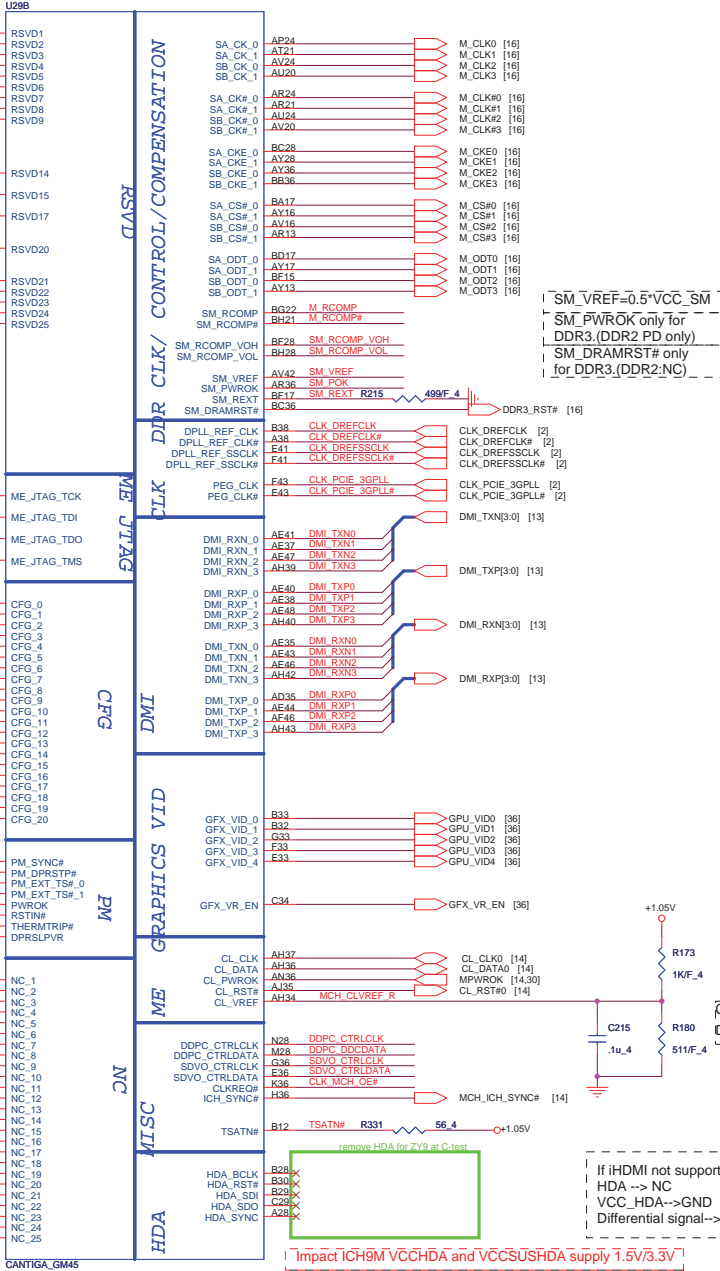
Strap table

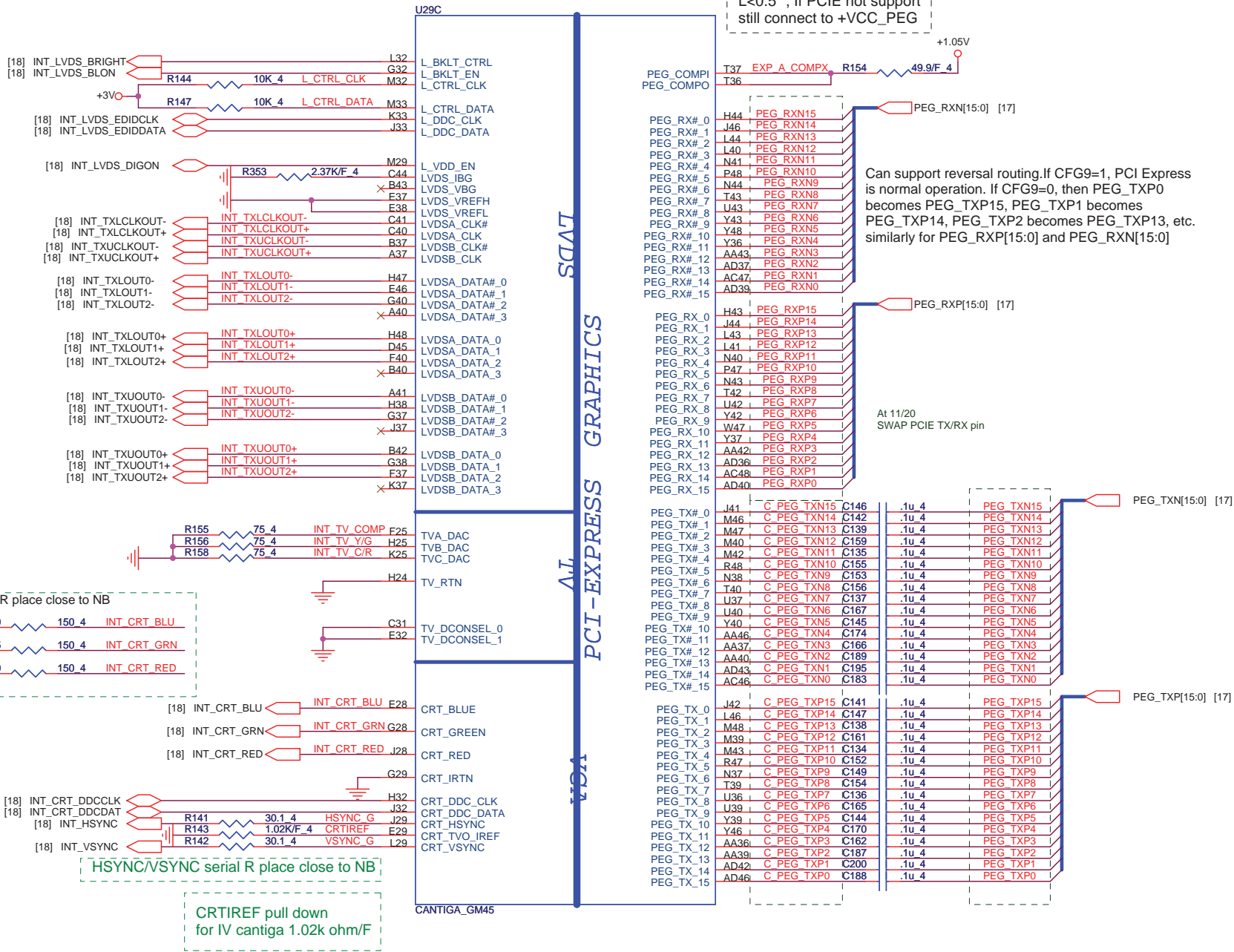
Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIe Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIe is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/iHDMI Device Present(Default) 1 = SDVO/iHDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

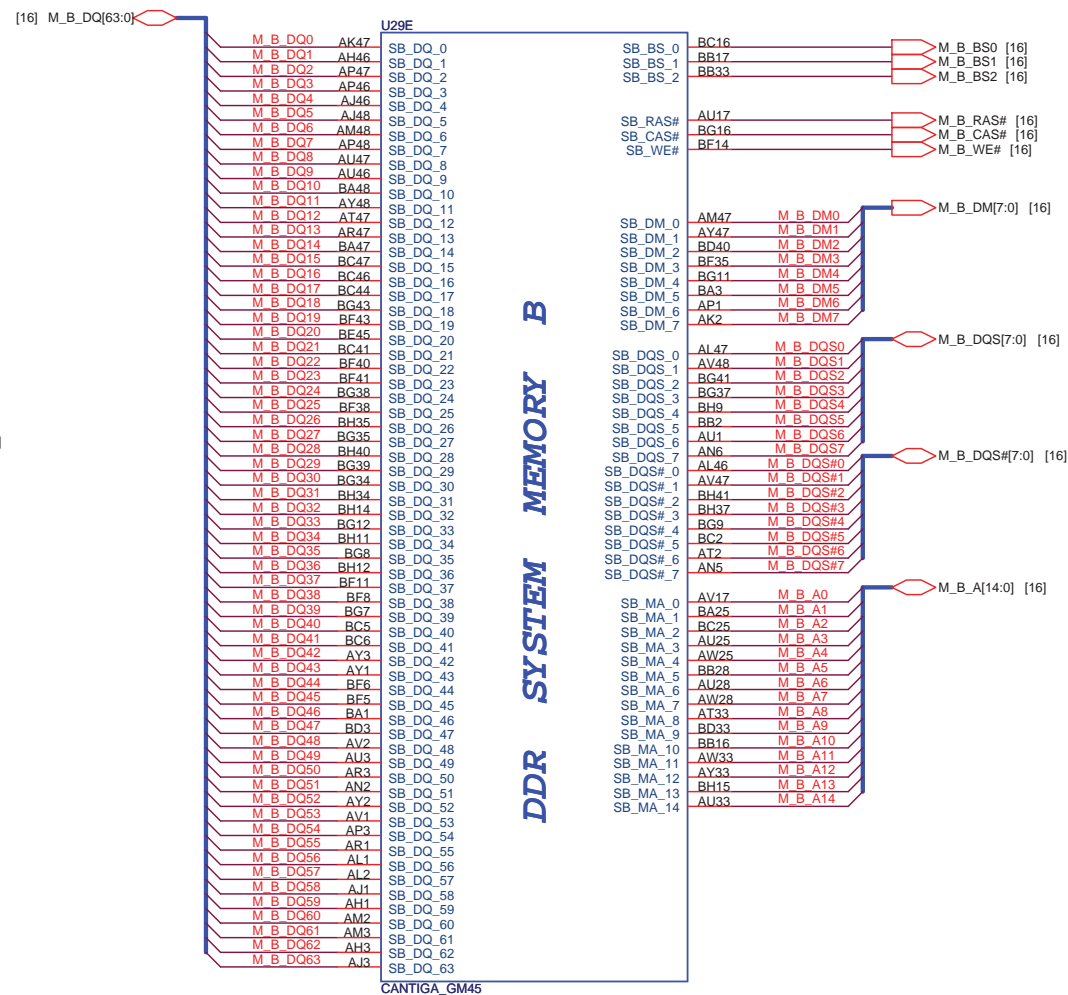
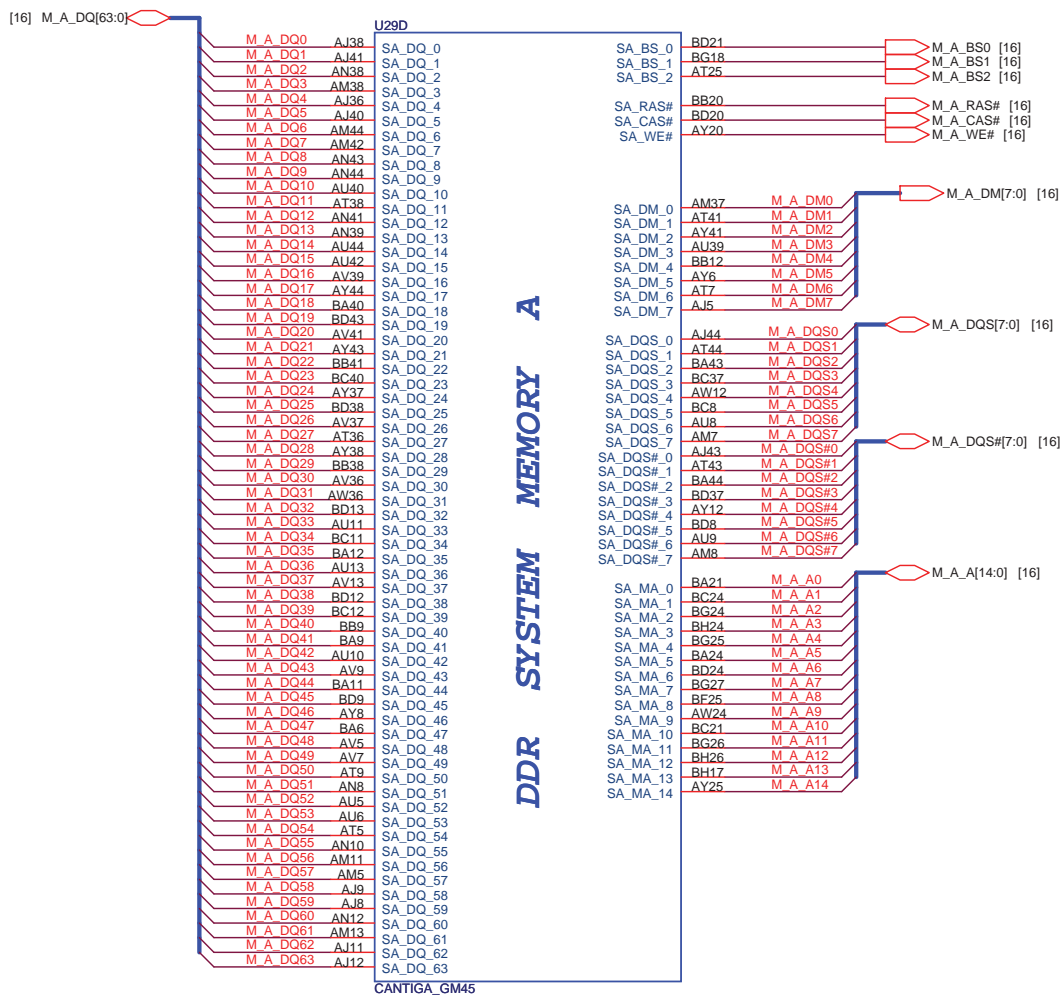
Strap pin




NB Thermal trip pin  
No use Thermal trip NB side can NC.(NB has ODT)  
PM DPRSTP#  
The Daisy chain topology should be routed from ICH9M to IMVP, then to (G)MCH and CPU, in that order.







GMCH (CANTIGA)

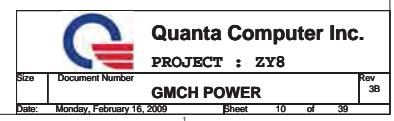


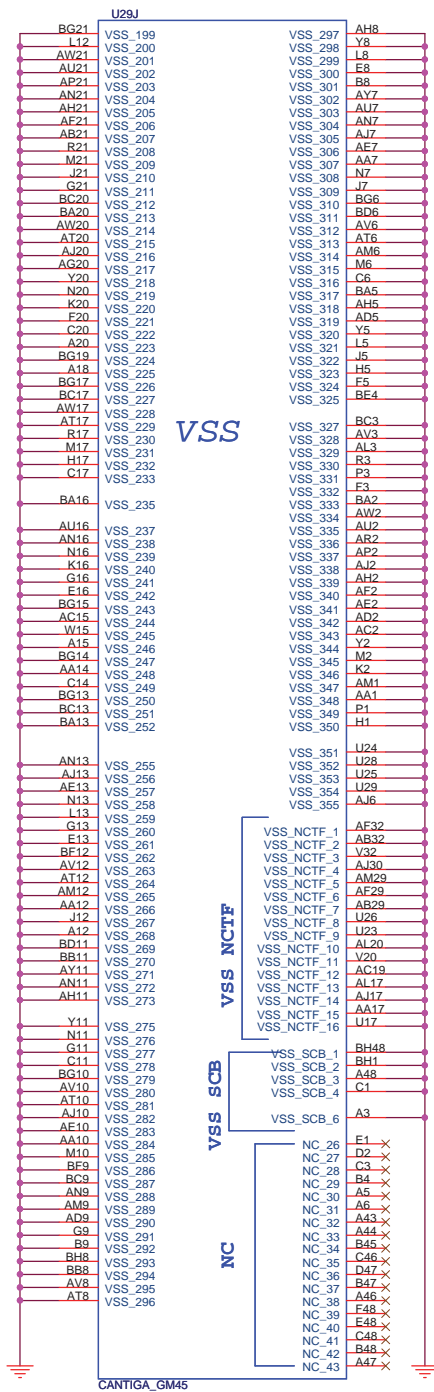
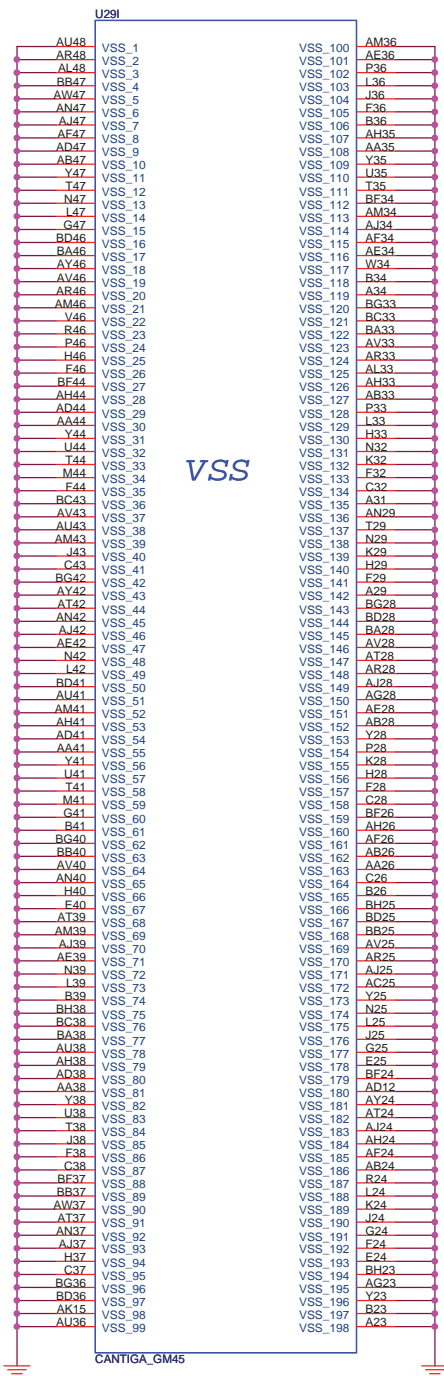
**Quanta Computer Inc.**  
**PROJECT : ZY8**

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		3B
<b>GMCH DDR I/F</b>		
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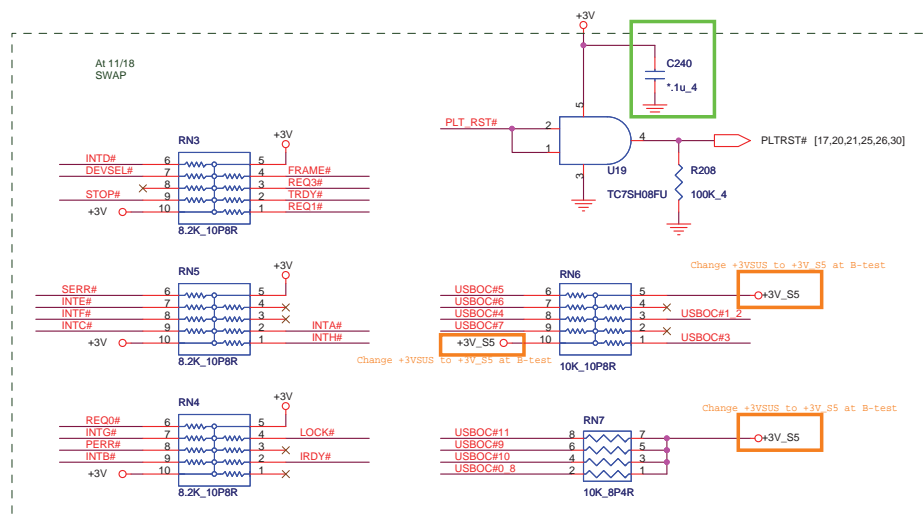




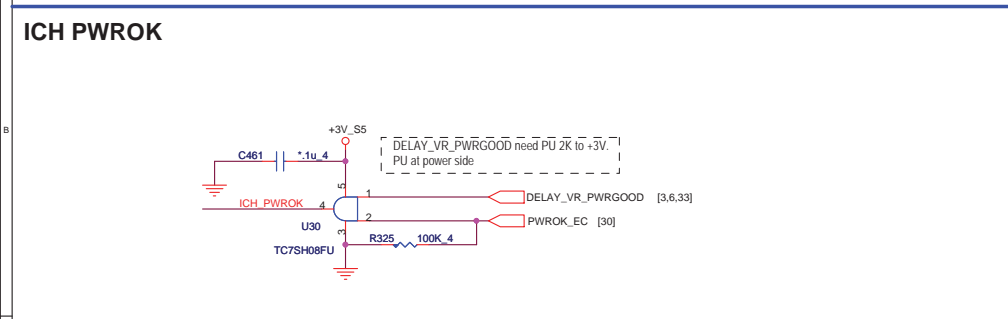
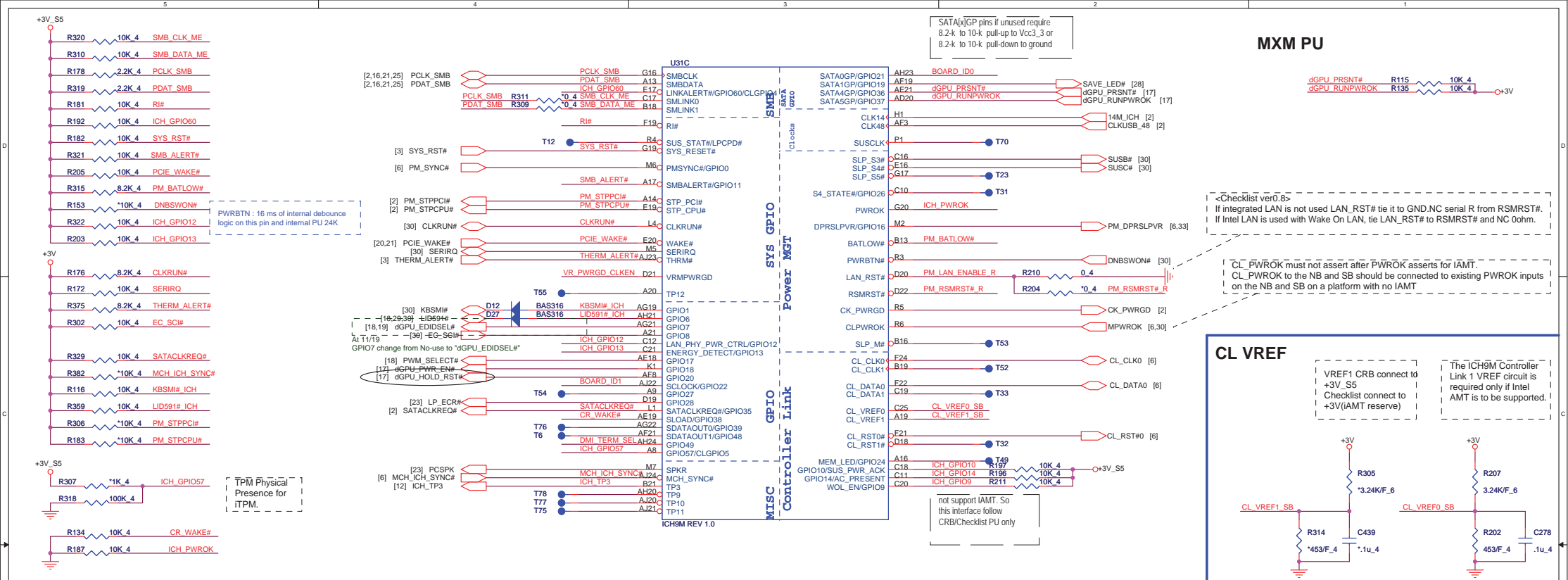




Pin Name	Strap description	Sampled	Configuration			PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0			
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default			
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default			
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default			
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable			
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0	SPI_CS#1	Boot Location	
			0	1	SPI	
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1	0	PCI	
			1	1	LPC(Default)	

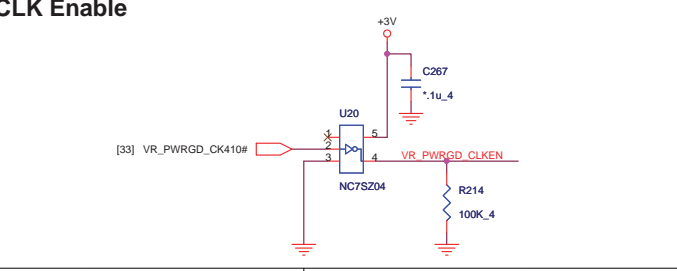
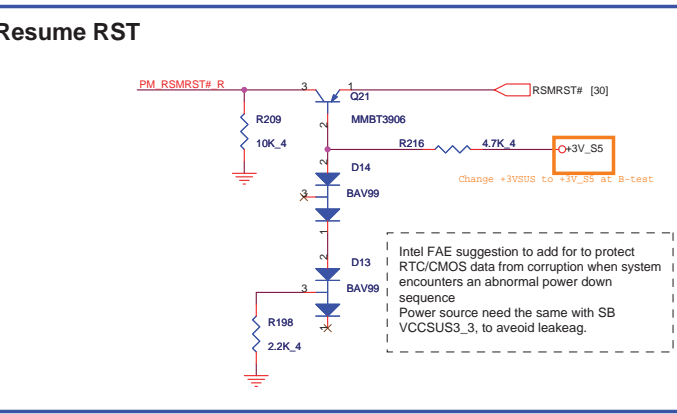






Board ID	ID2	ID1	ID0
default	0	0	0
	0	0	1
	0	1	0
	0	1	1
	1	0	0

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R166 *1K 4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R383 *1K 4



Board ID	ID2	ID1	ID0
default	0	0	0
	0	0	1
	0	1	0
	0	1	1
	1	0	0

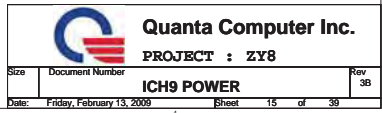
**Quanta Computer Inc.**

**PROJECT : ZY8**

**ICH9M GPIO**

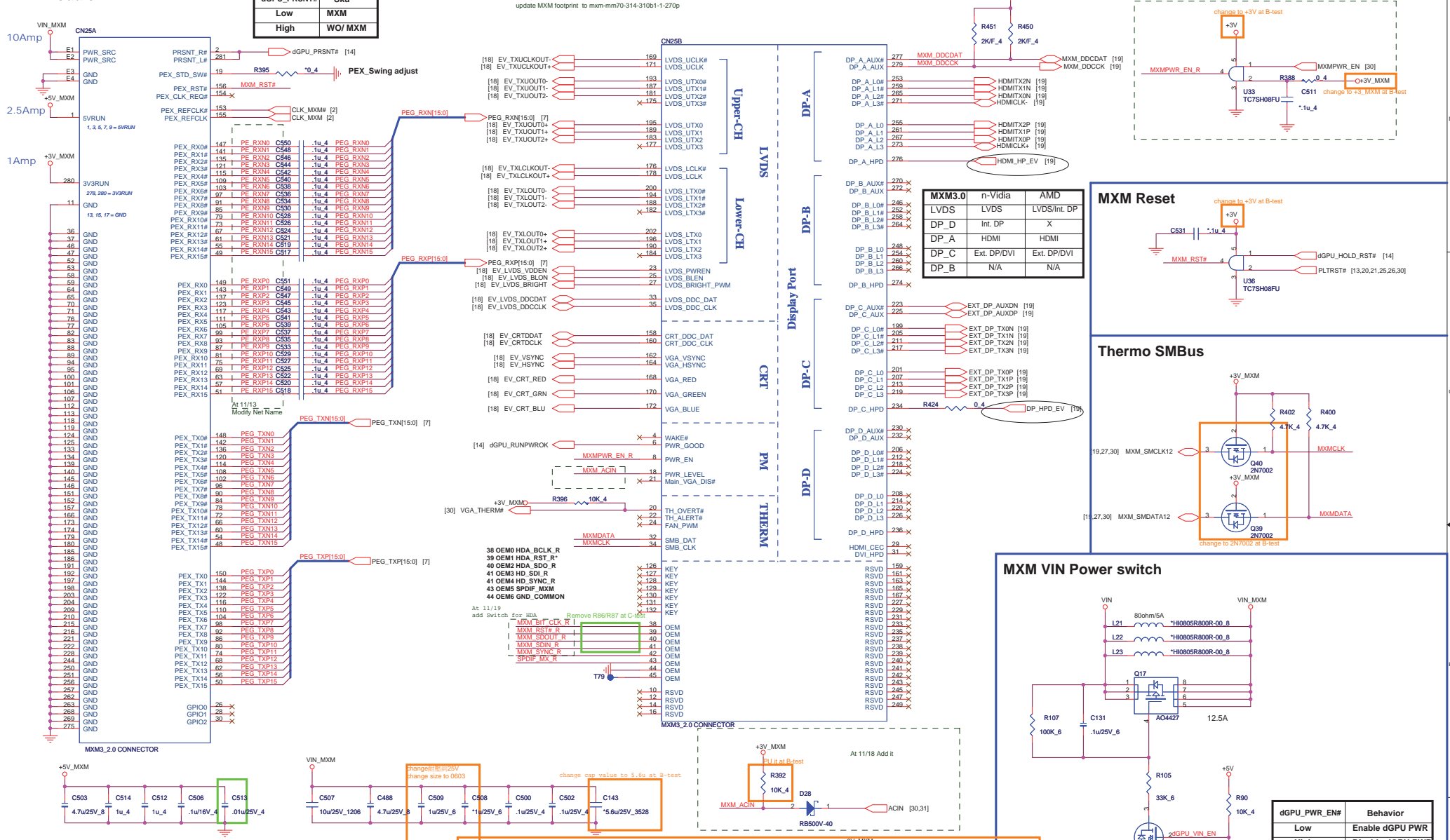
Size: Document Number: Rev: 3B

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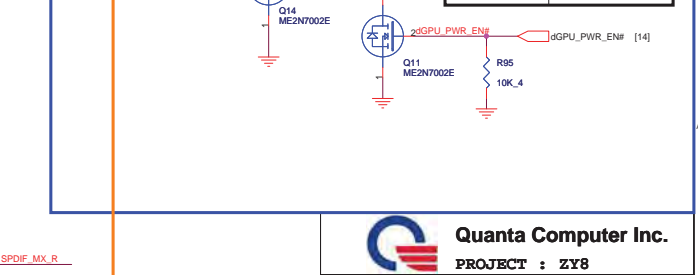
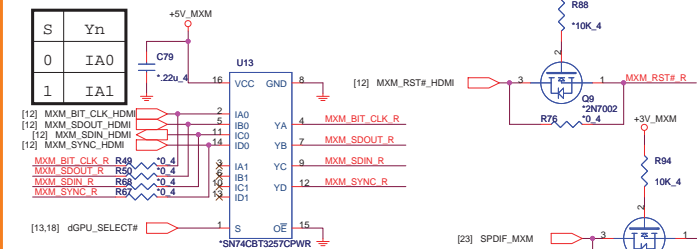
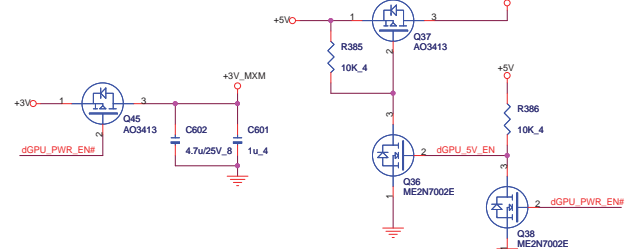




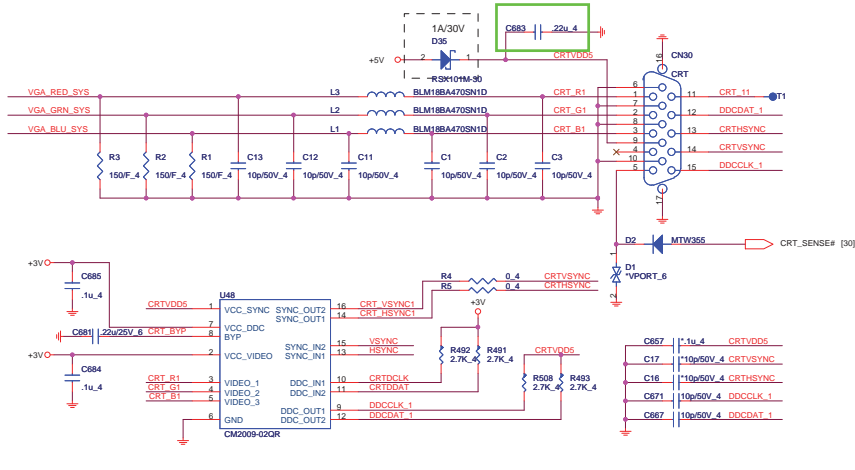
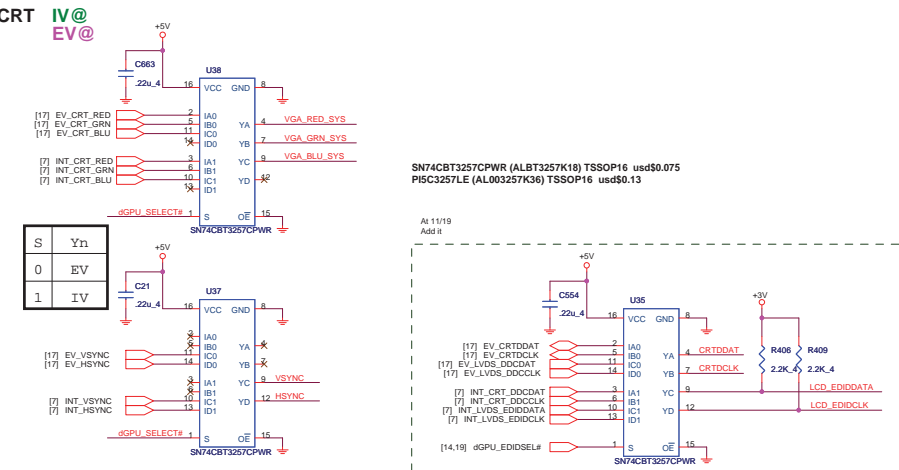
## MXM Module



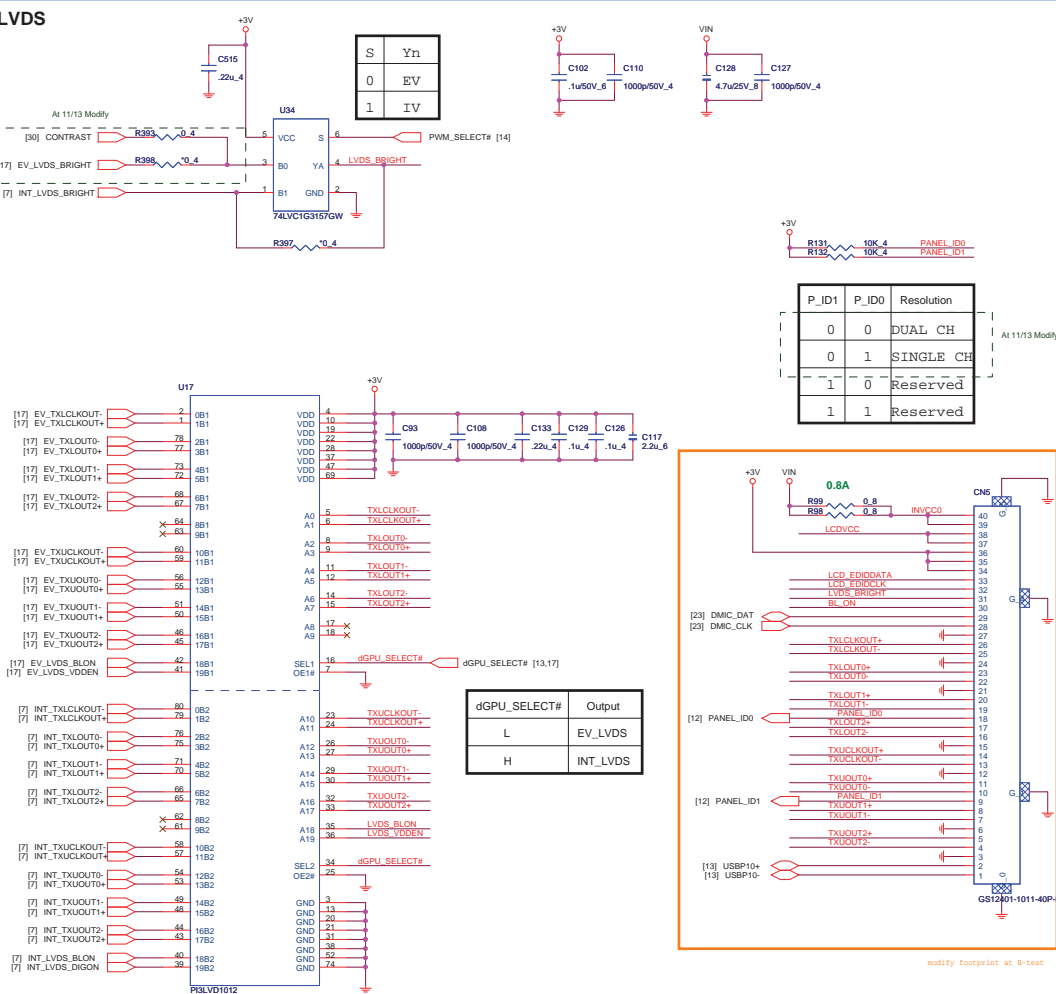
### MXM 3V/5V Power switch



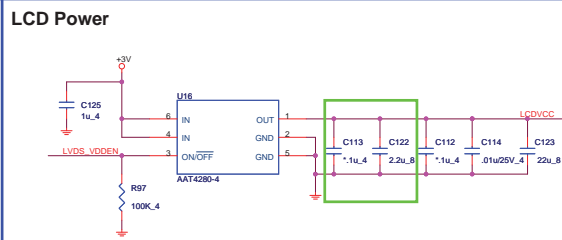
CRT  
IV@  
EV@



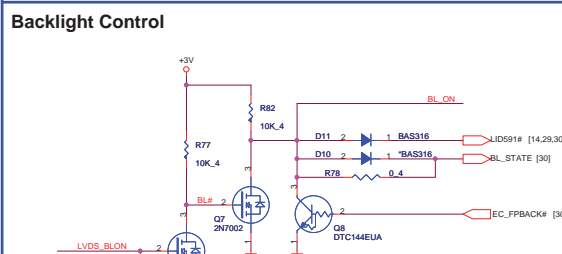
LVDS



LCD Power

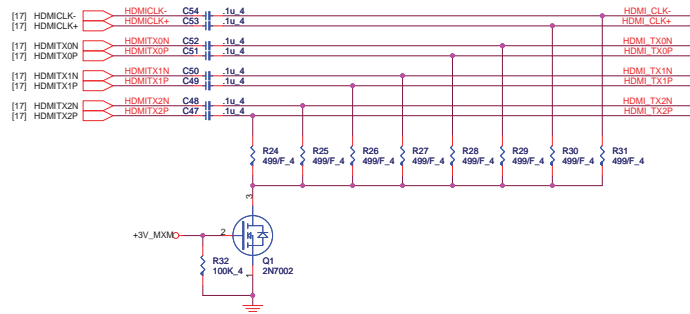


Backlight Control



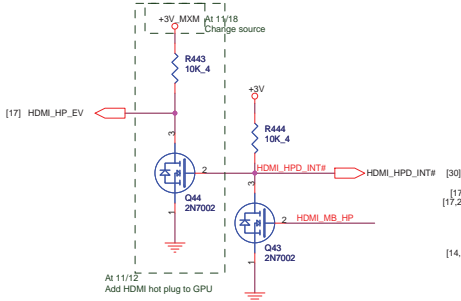
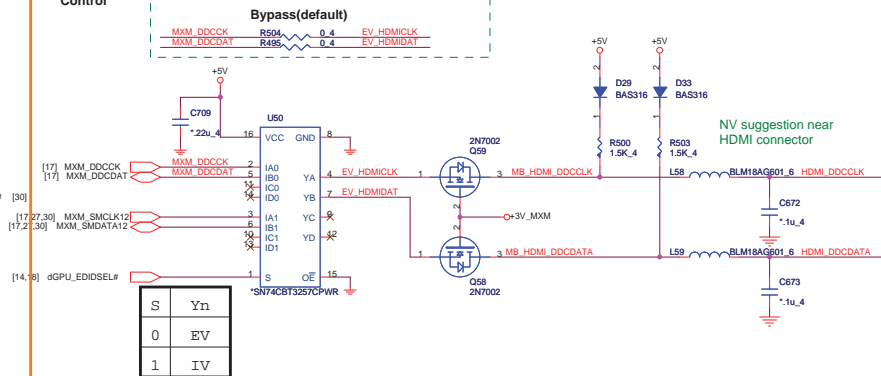


<b>HDMI</b>	TMDs (DC-coupled) DP (AC-coupled)
-------------	--------------------------------------

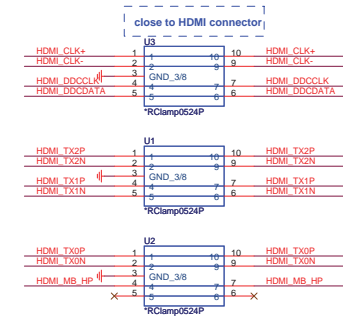


Close CN27

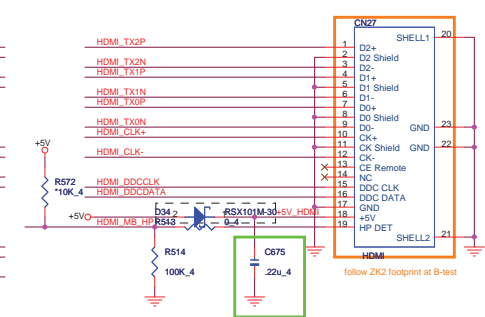
### HDMI Hot-PLUG to SB and GPU

SDVO I2C  
Control

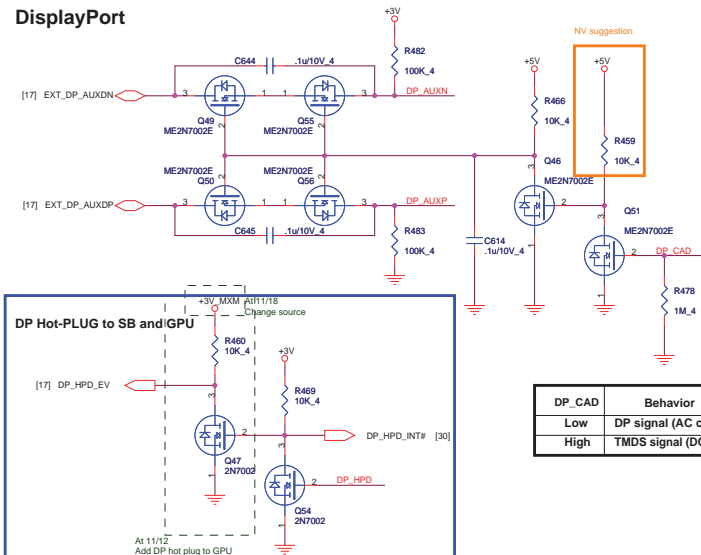
**ESD Protect**



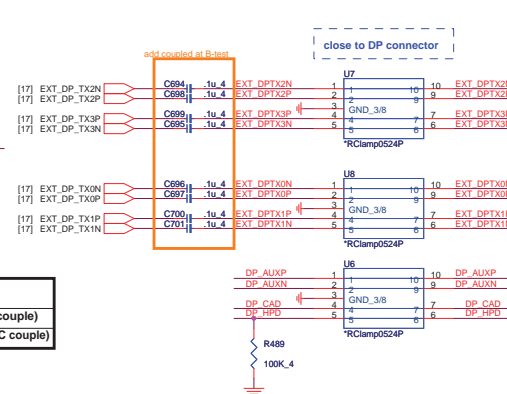
## HDMI connector



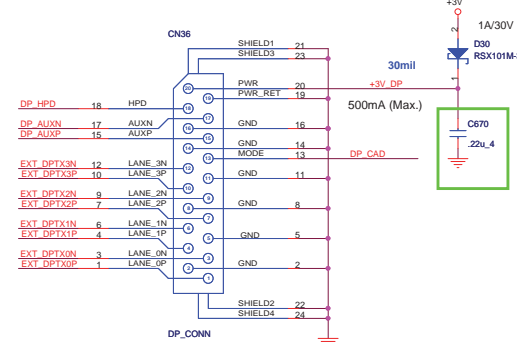
## DisplayPort



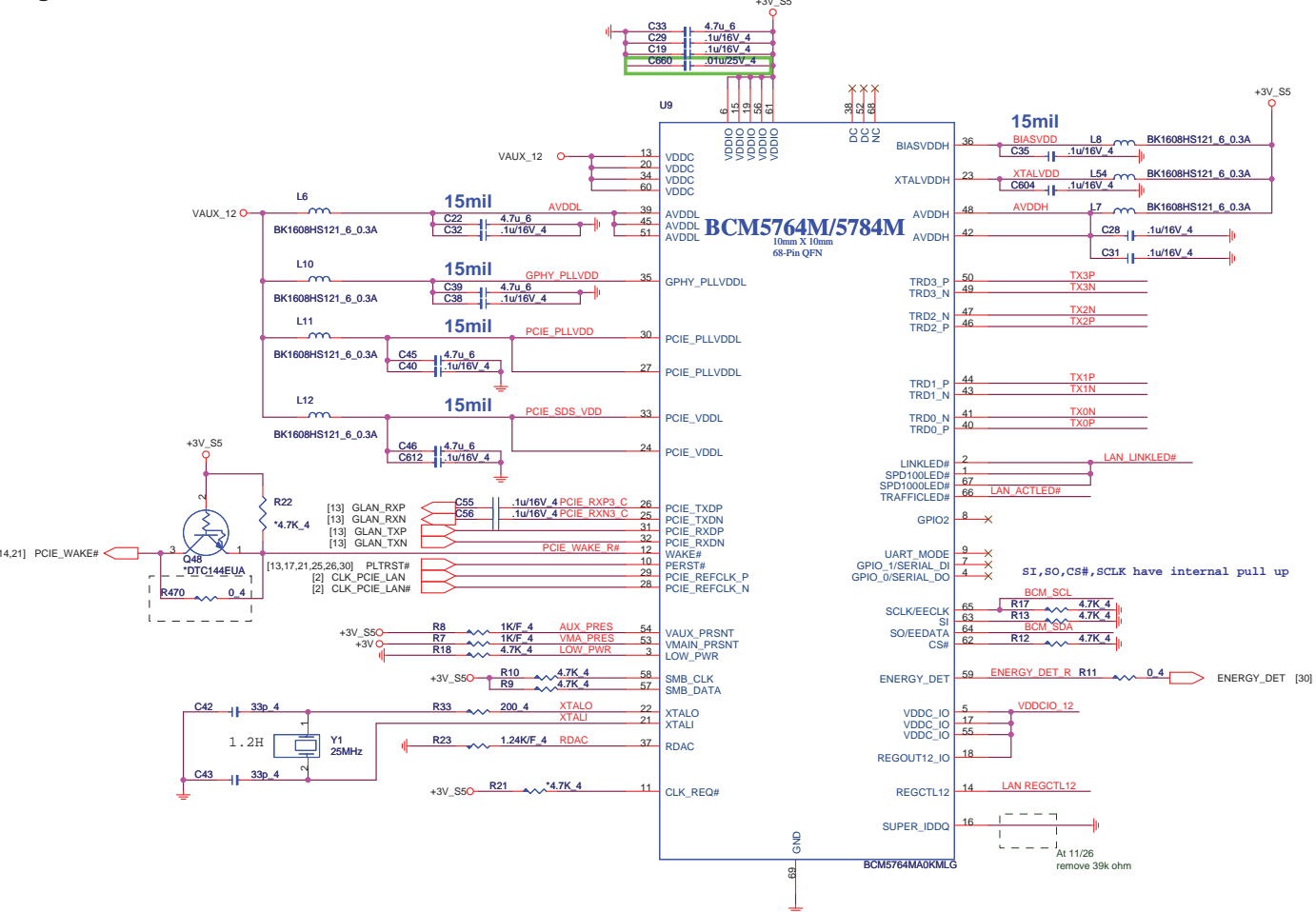
**ESD Protect**



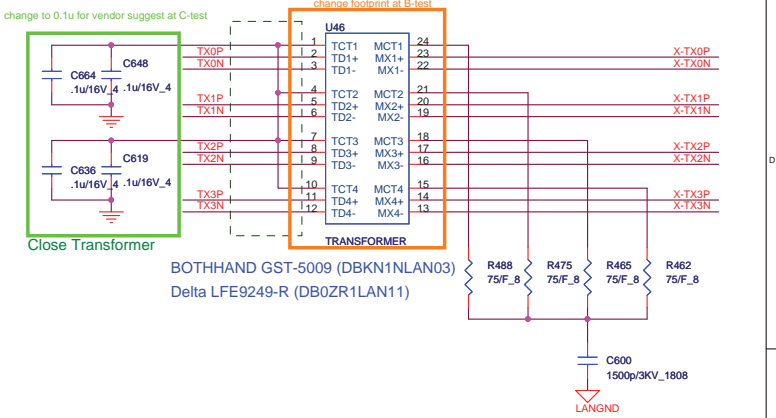
## DP connector DFHS20FR029



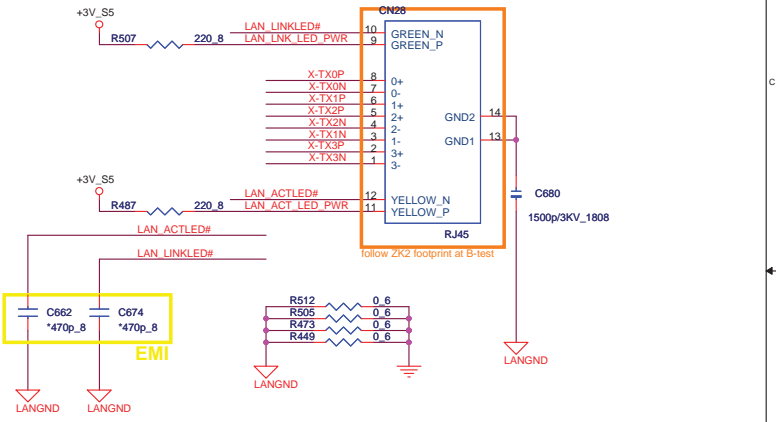
# Giga-LAN BCM5764M/5784M



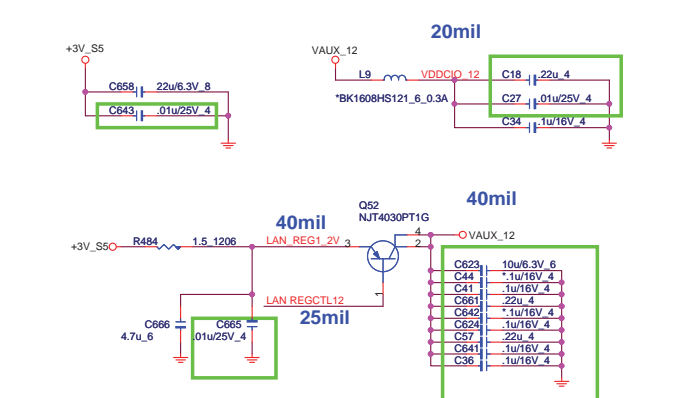
## TRANSFORMER



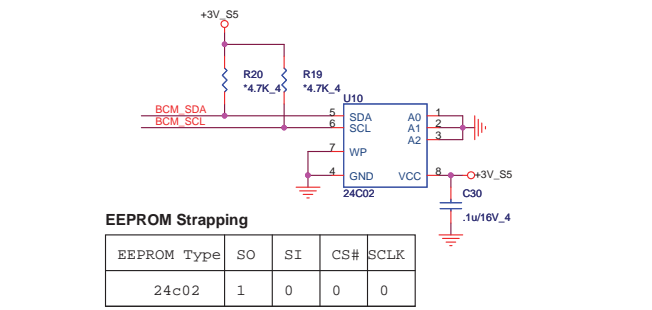
## RJ45



## LAN POWER



## EEPROM



EEPROM Strapping

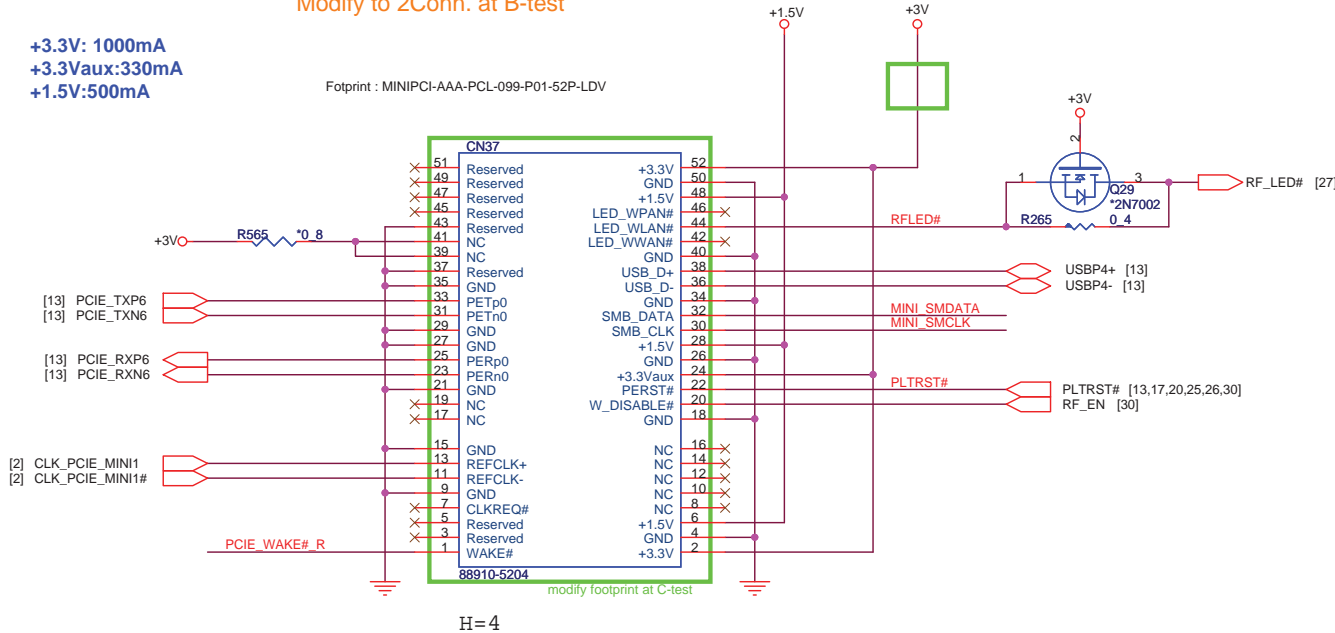
EEPROM Type	SO	SI	CS#	SCLK
24c02	1	0	0	0

# Wireless

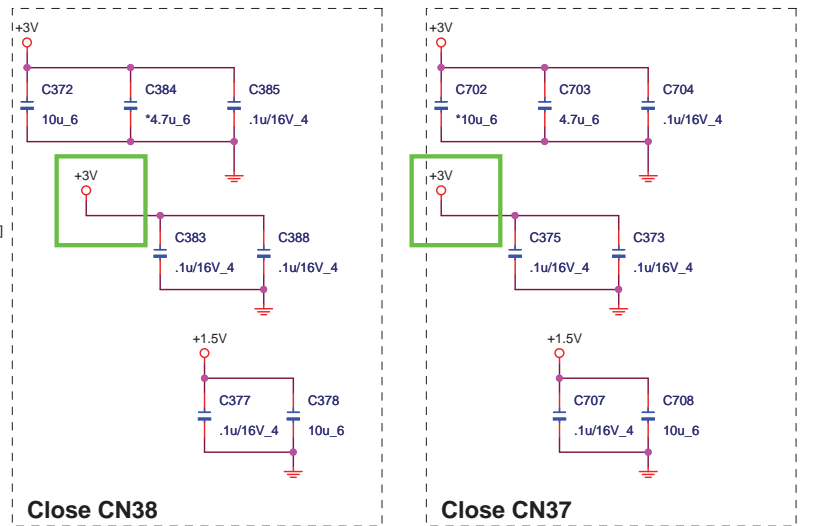
Modify to 2Conn. at B-test

+3.3V: 1000mA  
+3.3Vaux: 330mA  
+1.5V: 500mA

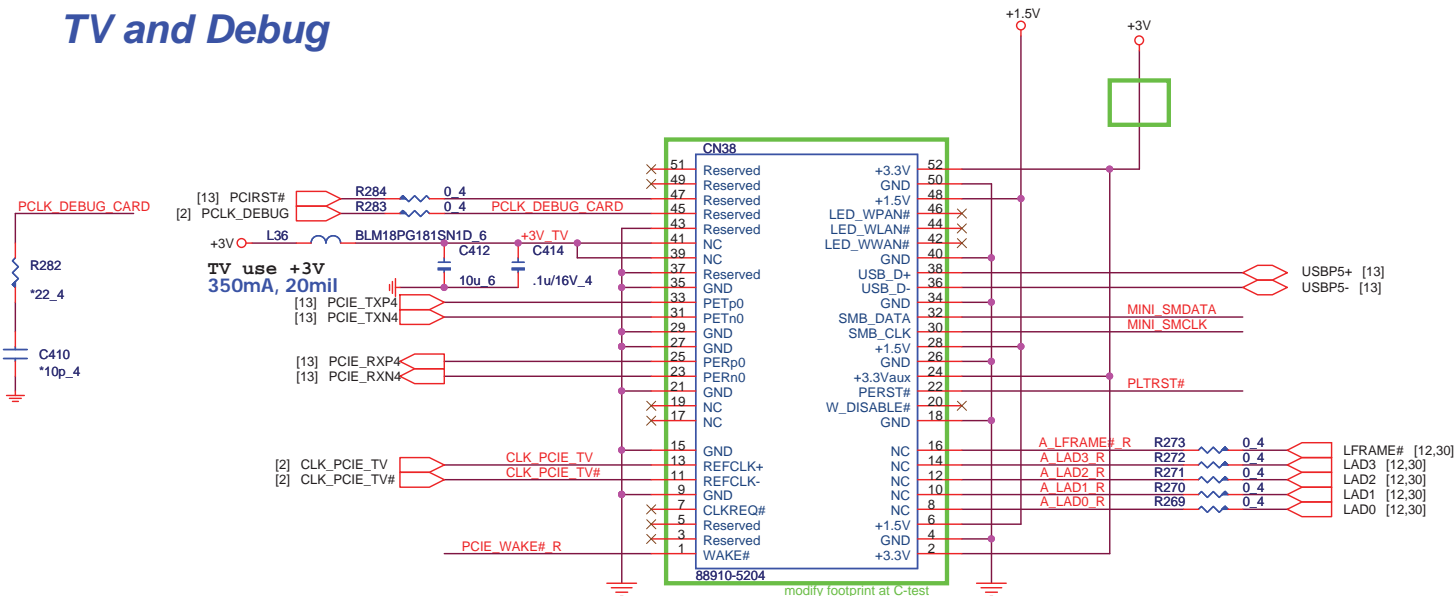
Fotprint : MINIPCI-AAA-PCL-099-P01-52P-LDV



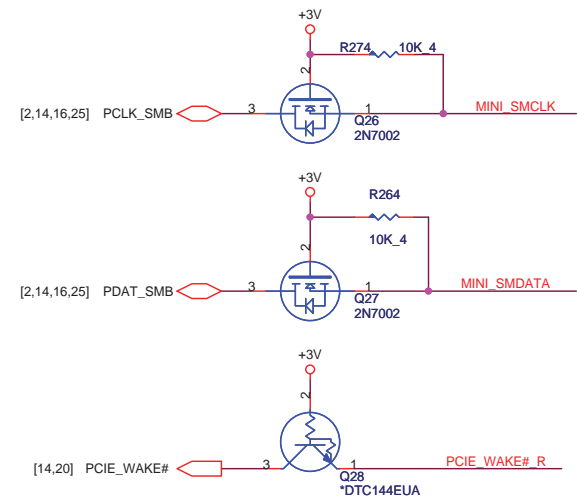
H=4



# TV and Debug



H=9



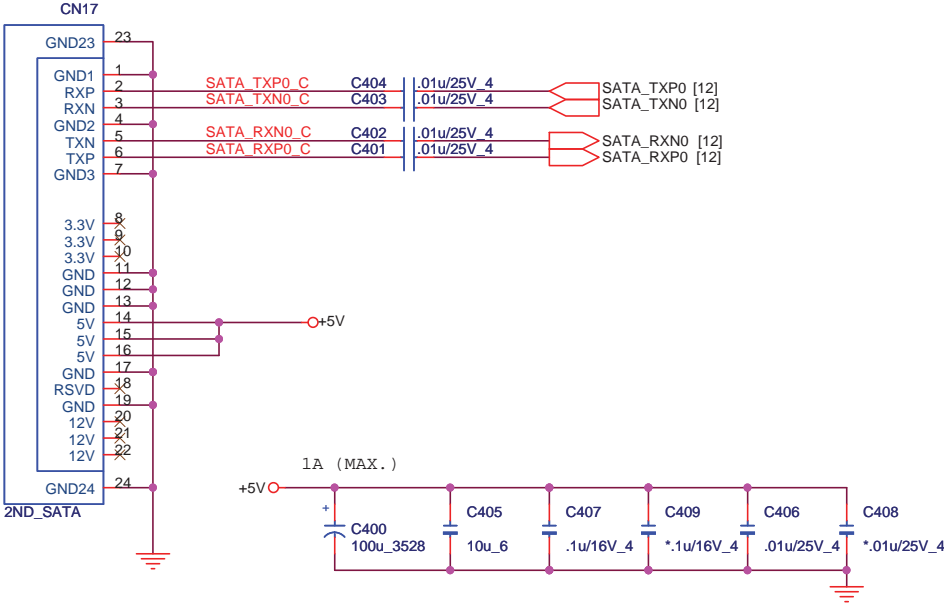
**Quanta Computer Inc.**

**PROJECT : ZY8**

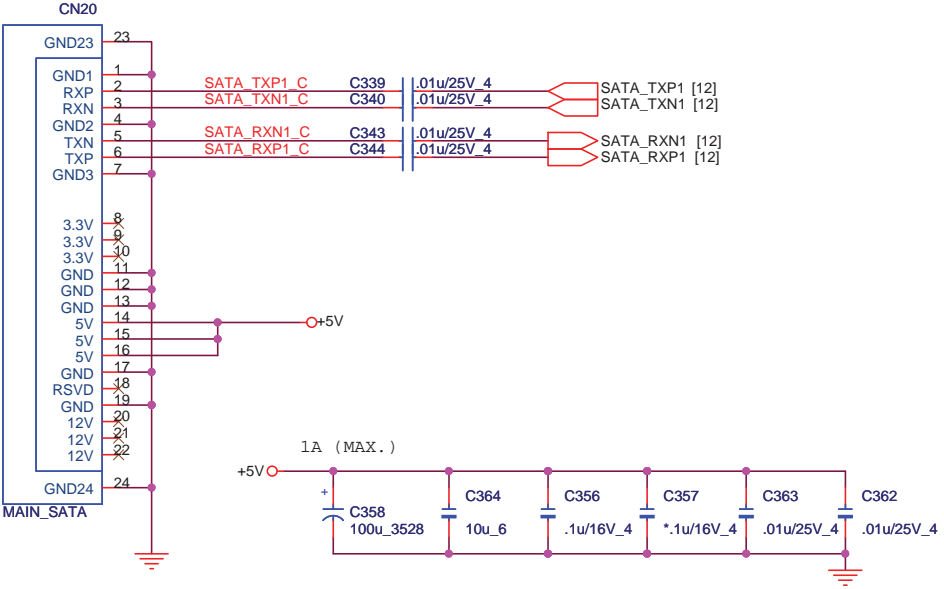
**MINI PCI-E card/TV**

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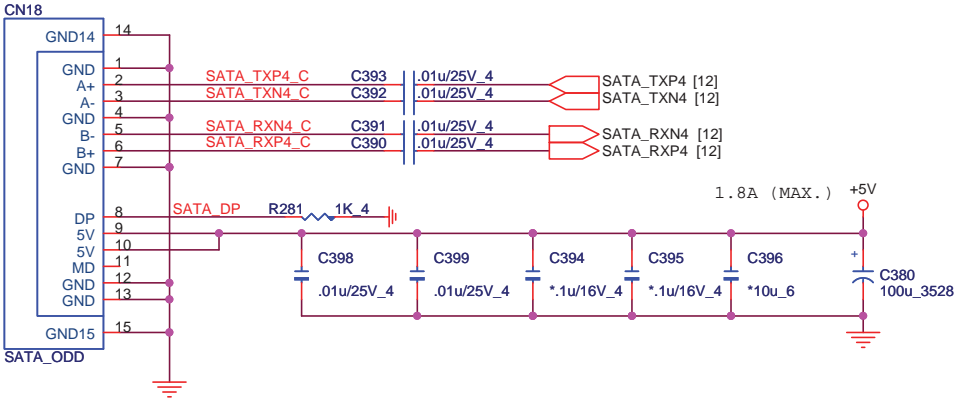
2nd SATA HDD (edge of board)



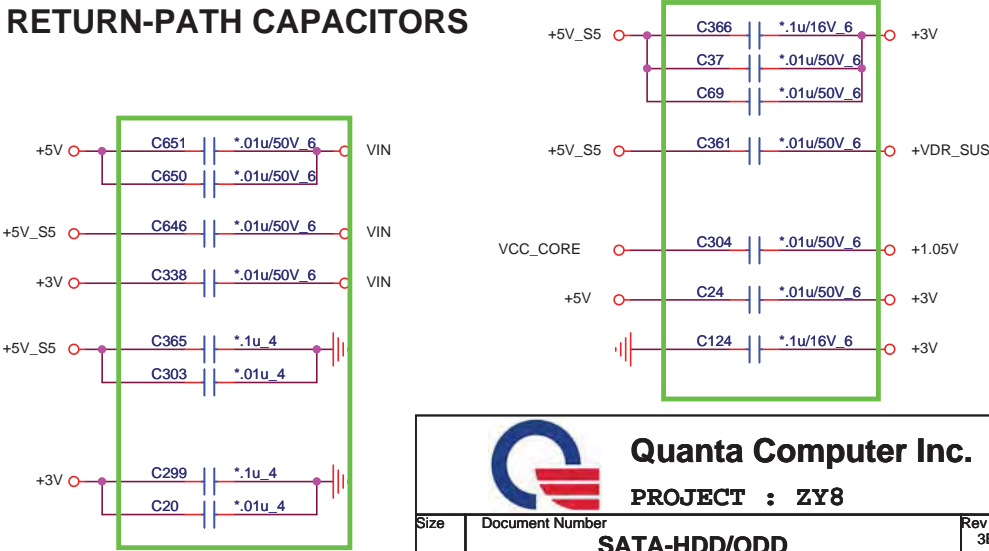
MAIN SATA HDD




ODD (SATA)



EE RETURN-PATH CAPACITORS





**Quanta Computer Inc.**  
**PROJECT : ZY8**  
**SATA-HDD/ODD**

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		3B
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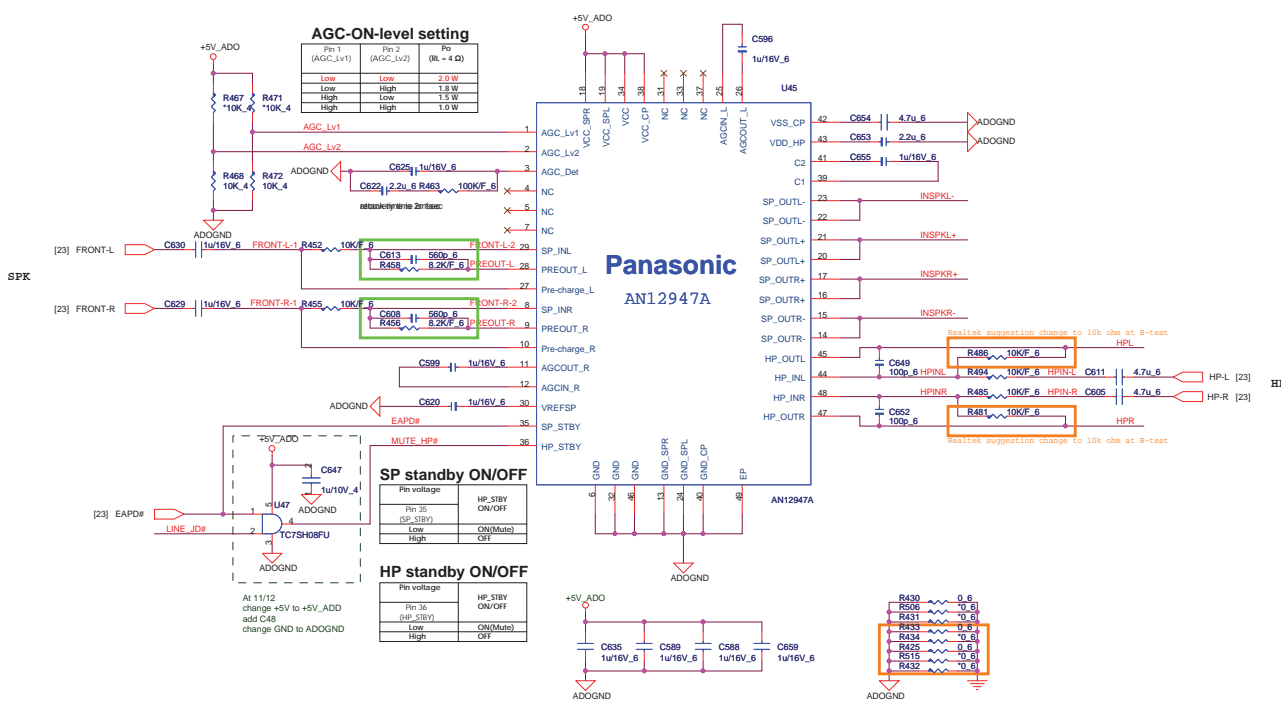
IV@  
EV@



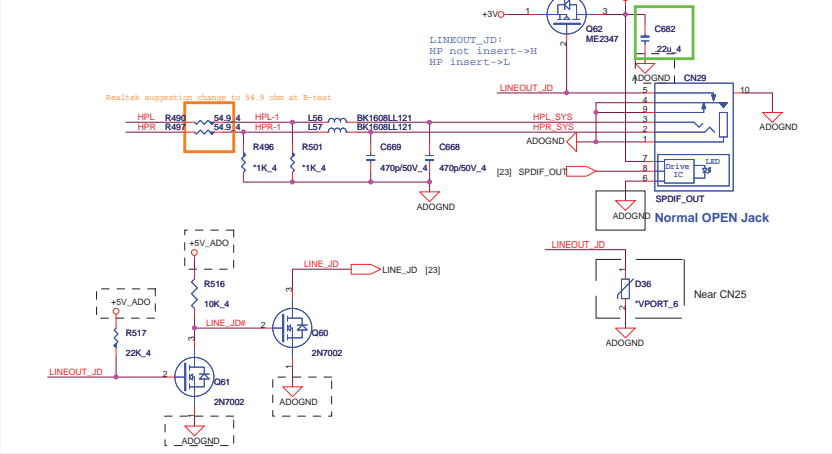
At 11/13  
change GND to ADOGND



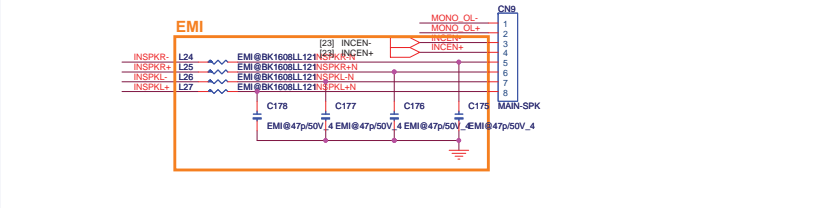
SPEAKER/HP AMP.



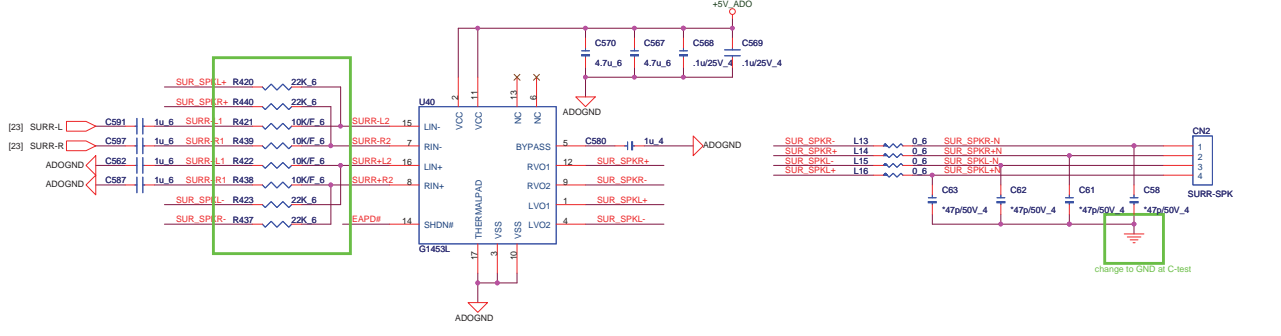
LINE-OUT/SPDIFO



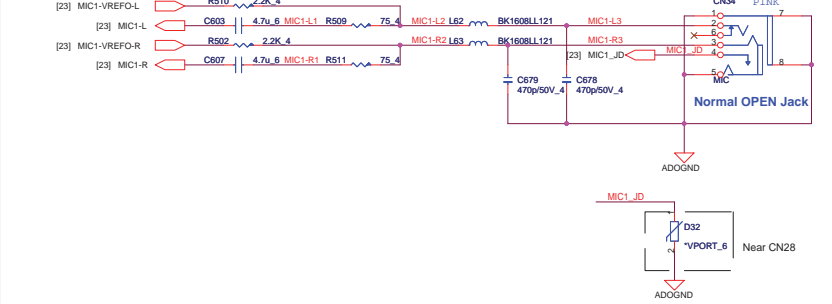
Main SPK/Center/Subwoofer



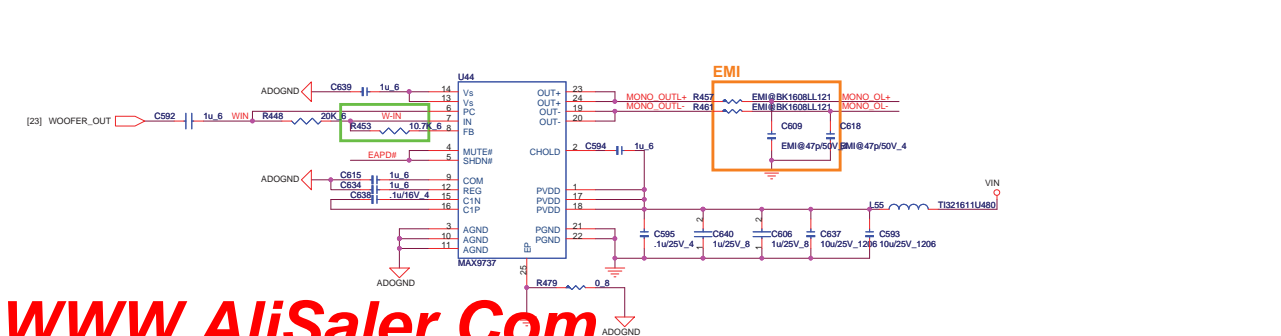
SURR-SPK



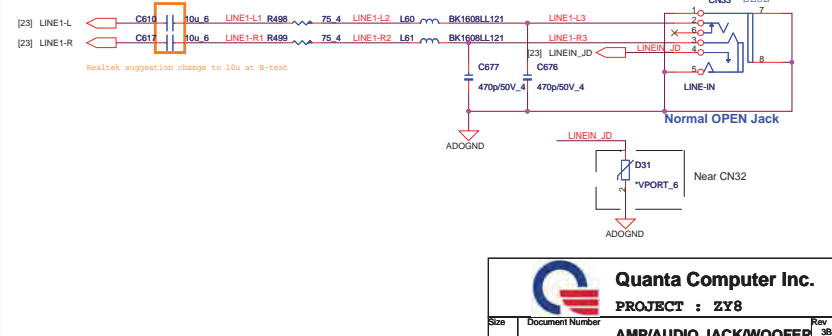
MIC



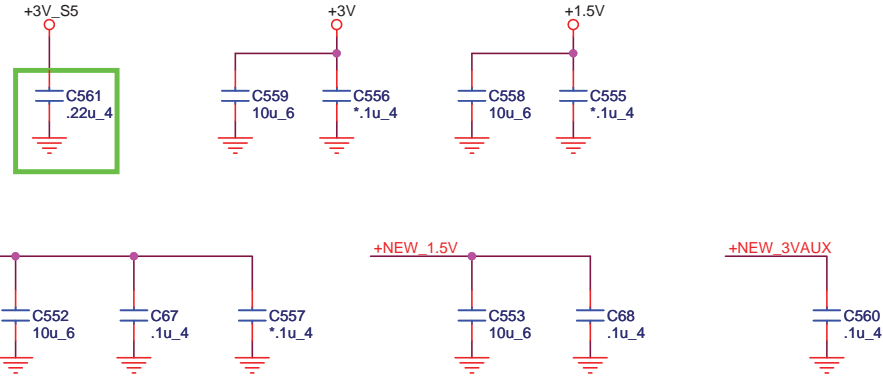
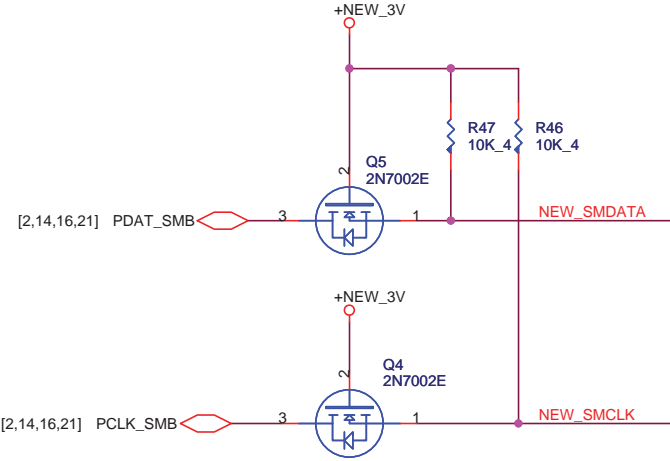
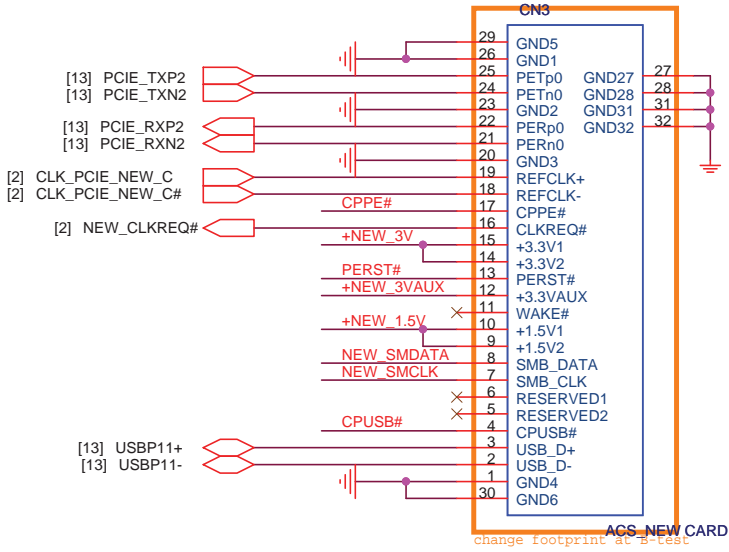
SUBWOOFER



LINE IN



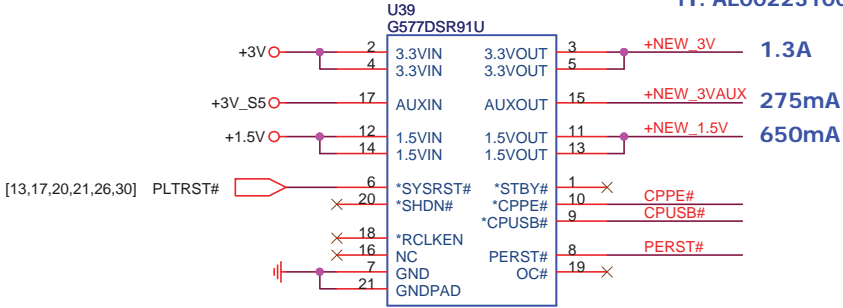
NEW CARD




NEW CARD'S POWER SWITCH

At 11/18  
Change GMT cost down version.

GMT: AL000577002  
TI: AL002231000





**Quanta Computer Inc.**  
PROJECT : ZY8

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NEW CARD		
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## change Cardreader to OZ88GS0LN at B-test

[illegible]

TPBIAS0

C71 1uF\_4

R60 56.2F\_4

R59 56.2F\_4

At 11/24 SWAP

L5

\*1394@CL-2M2012-121JT

RN2 0X2\_4

L1394 TPA0+

L1394 TPA0-

TPA0P

TPA0N

TPB0N

TPB0P

RN1 0X2\_4

L1394 TPB0+

L1394 TPB0-

R57 56.2F\_4

R58 56.2F\_4

1394\_COM

R51 5.1kF\_4

C70 270p/25V\_4

CN35

1394 Conn

L1394 TPB0+

L1394 TPB0-

L1394 TPA0+

L1394 TPA0-

D3 \*1394@EGA L1394 TPB0-


D6 \*1394@EGA L1394 TPA0-

D5 \*1394@EGA L1394 TPA0+

D4 \*1394@EGA L1394 TPB0+

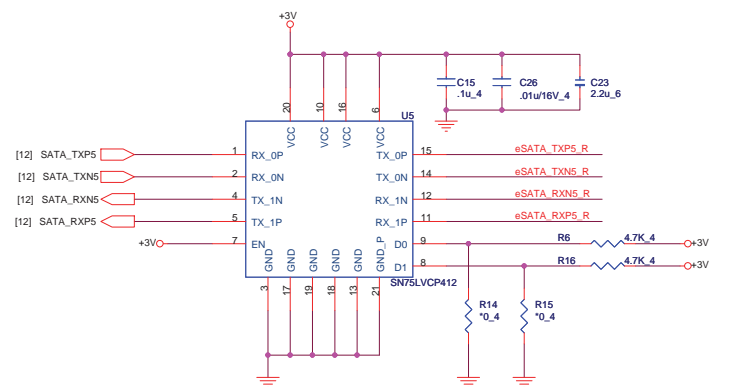
As close as possible to OZ888GS01N

modify footprint at B-test

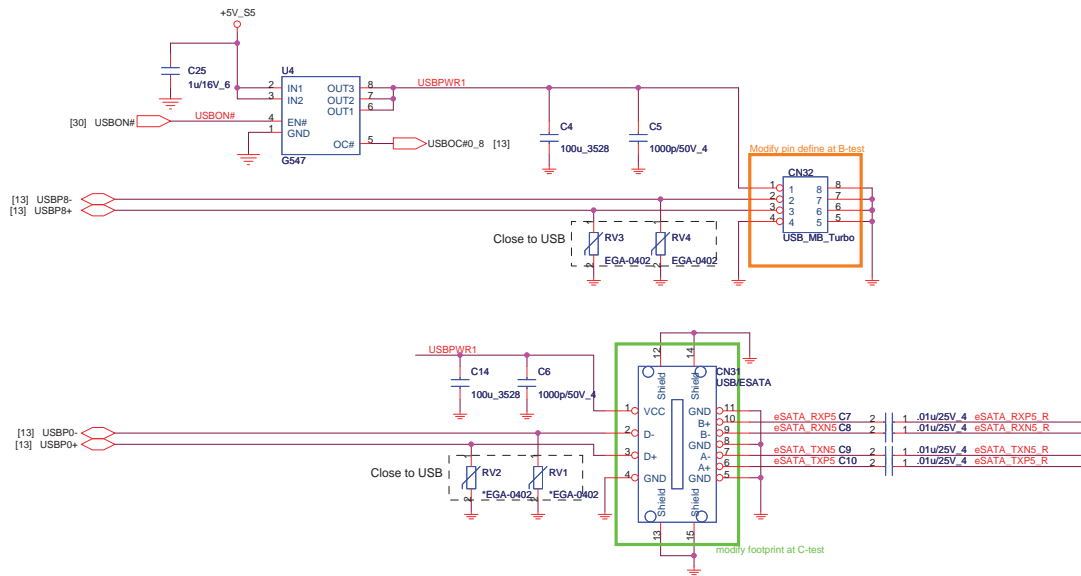
 <div> <b>Quanta Computer Inc.</b>  <b>PROJECT : ZY8</b> </div>		Rev
Size	Document Number	3B
<b>OZ888GS0L1N</b>		
Date:	Friday, February 13, 2009	Sheet 26 of 39



## USB & ESATA

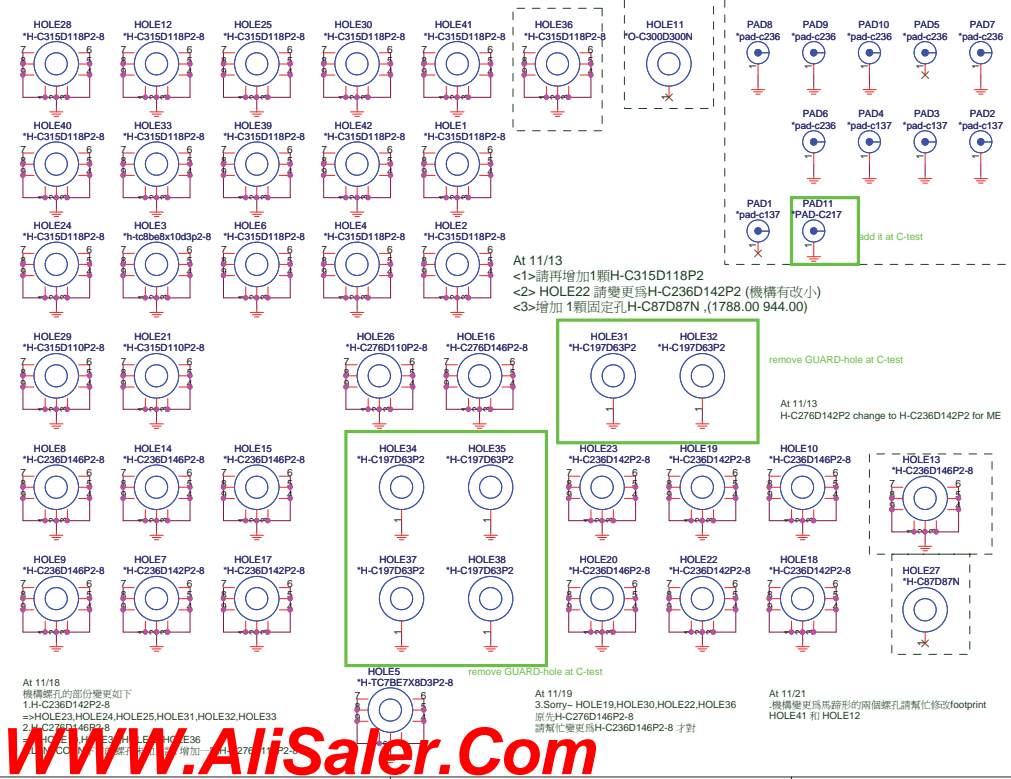


EN	D0	D1	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (5dB)	0dB
1	0	1	0dB	Pre-emphasis (5dB)
1	1	1	Pre-emphasis (5dB)	Pre-emphasis (5dB)

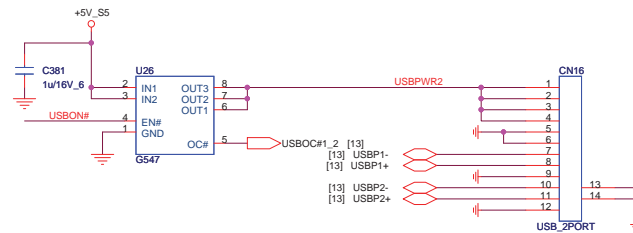


## HOLES

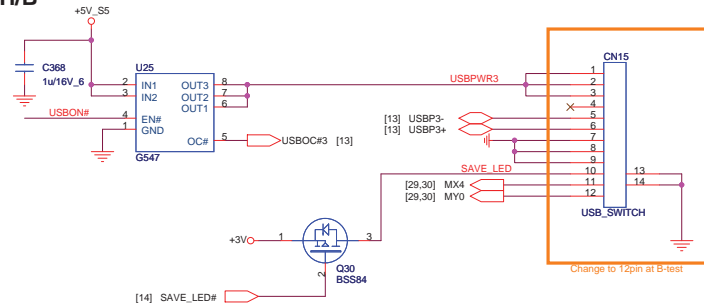
At 11/13  
change HOLE1-38 1PIN to 9PIN



## USB\_2PORT/B



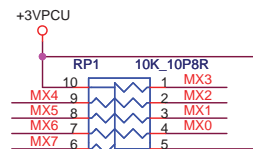
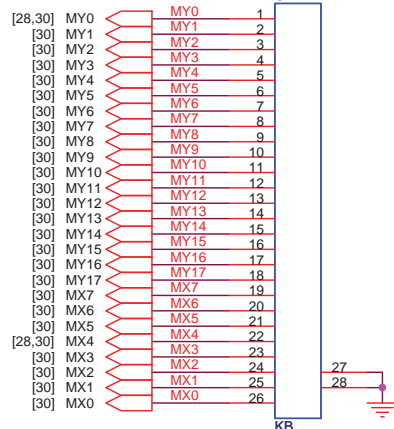
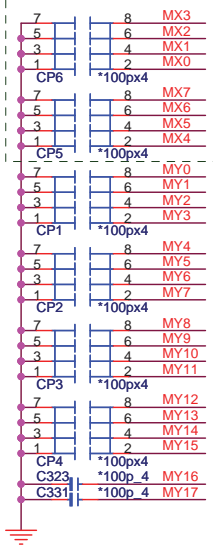
## USB\_SWITCH/B





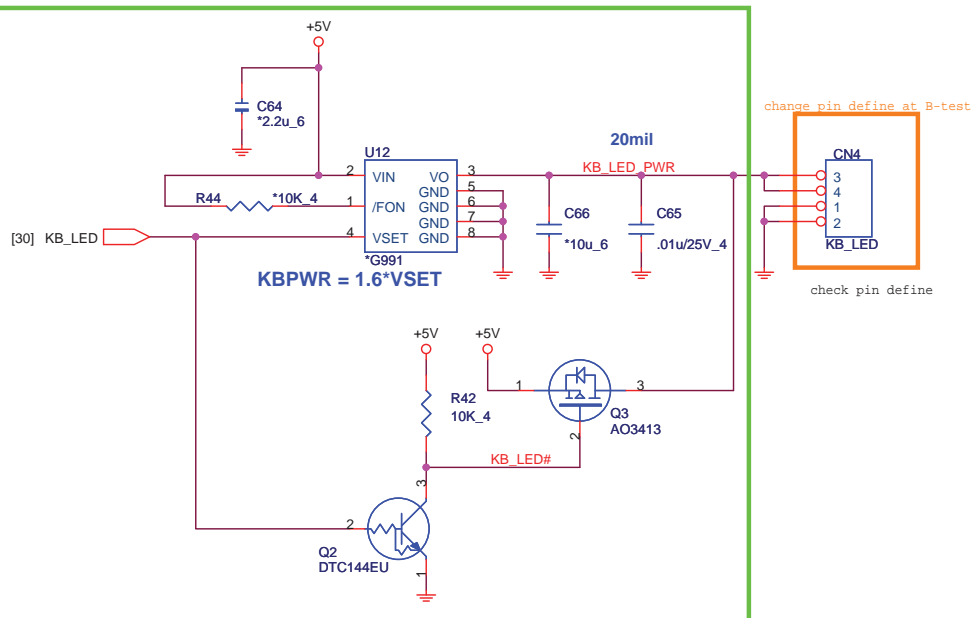
**INT\_K/B**

At 11/18  
SWAP

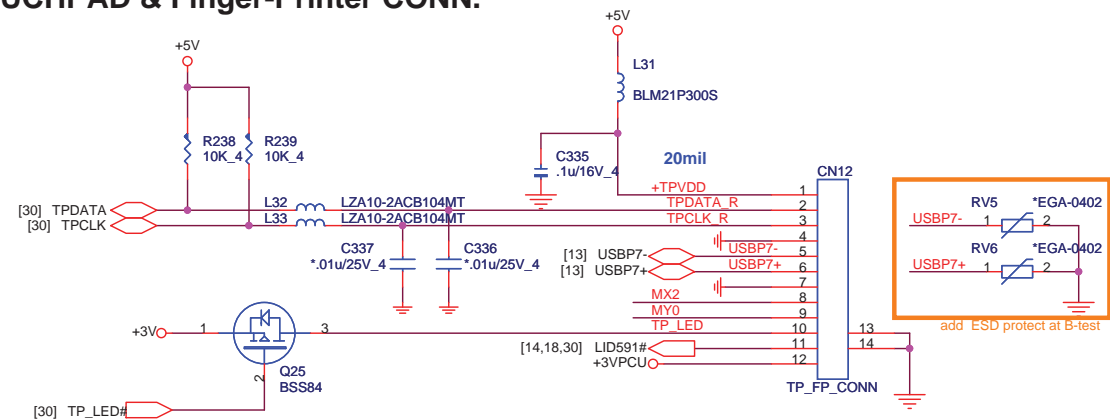


## Keyboard LED control

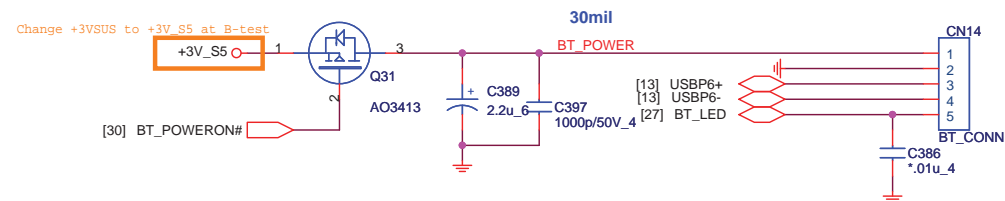
Remove: U12, C64, R44, C66.  
Stuff: Q3, R42, Q2  
at C-test



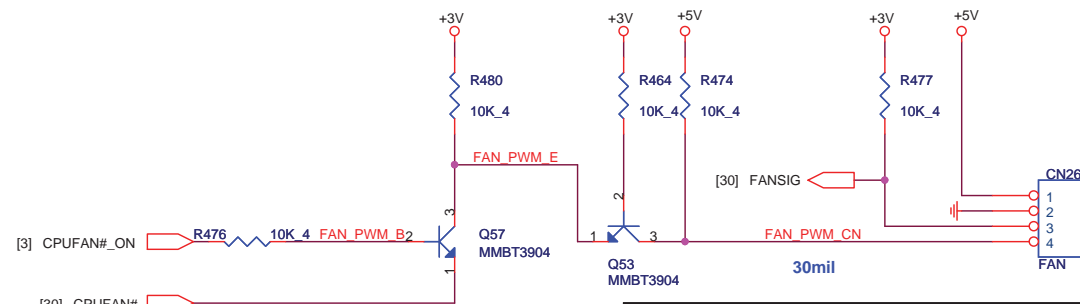
## TOUCHPAD & Finger-Printer CONN.



## BLUETOOTH CONNECTOR



## CPU FAN

**Quanta Computer Inc.**

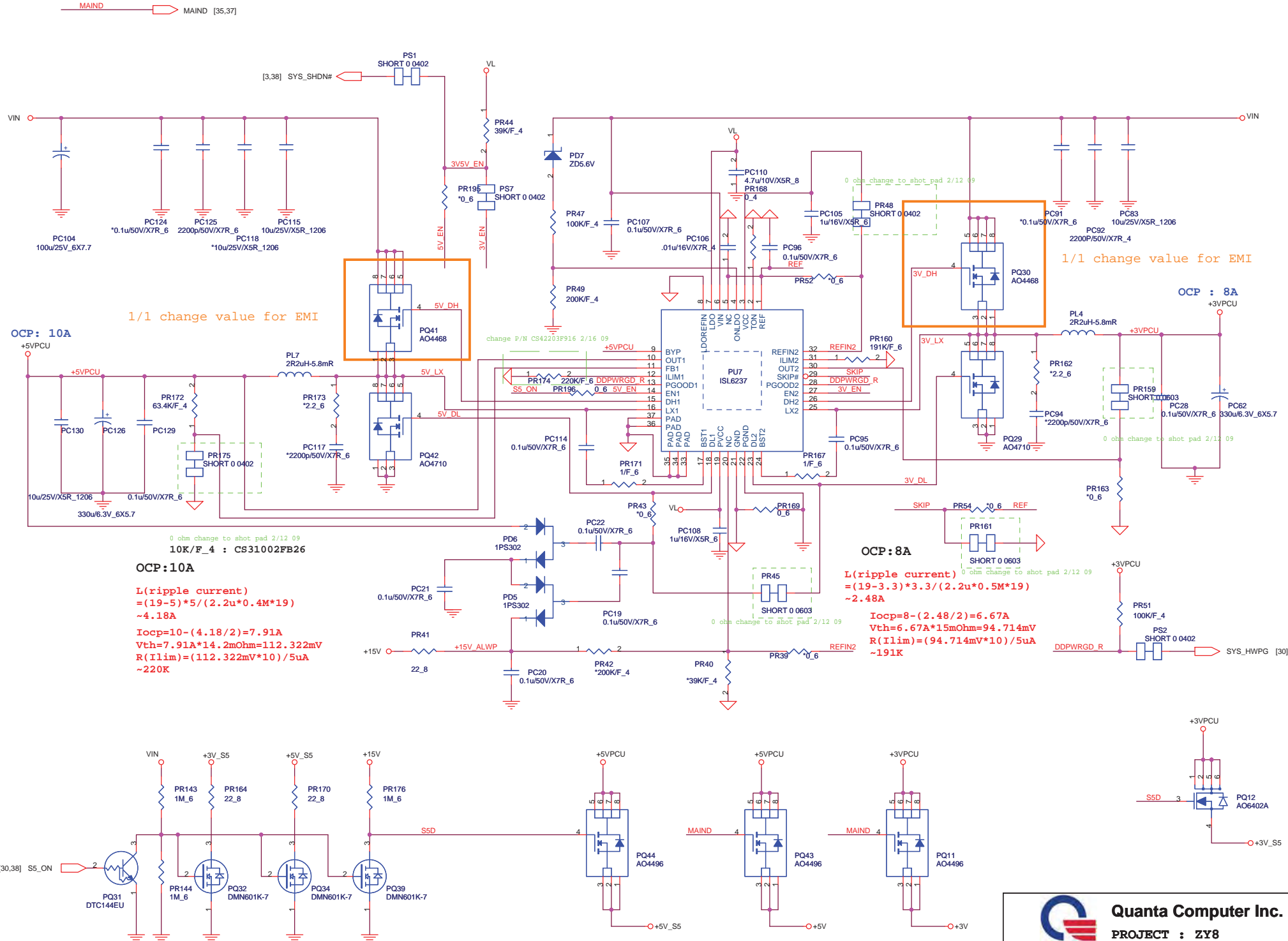
**PROJECT : ZY8**

**KB/FAN/TP+FP/BT**

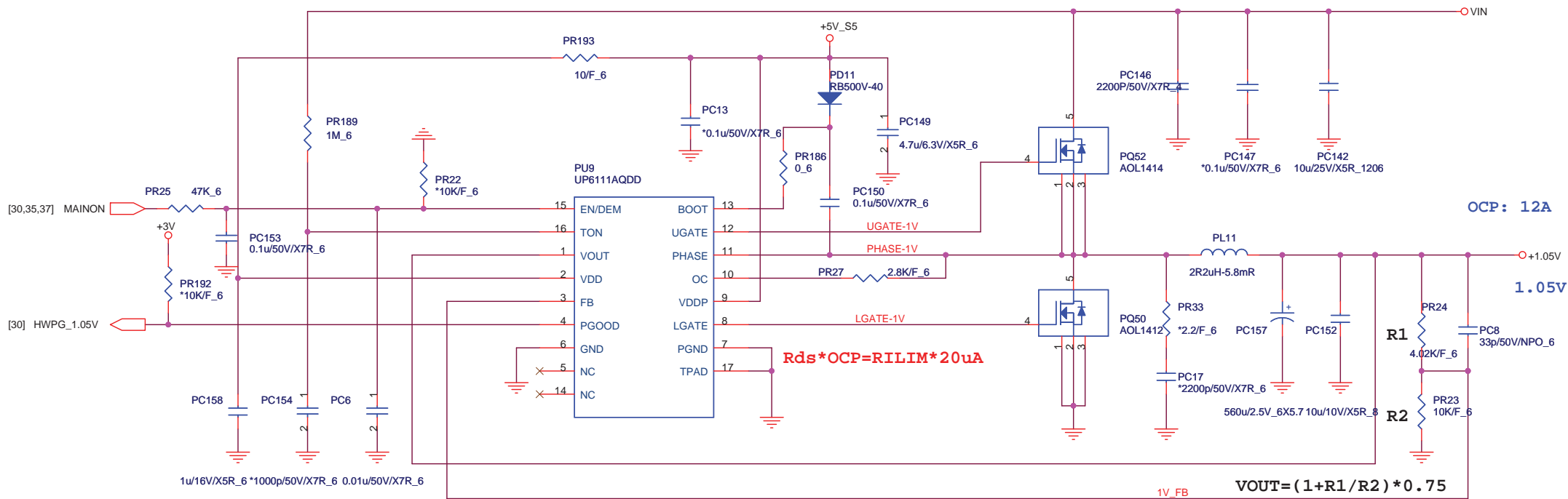
Size	Document Number	Rev
	<b>KB/FAN/TP+FP/BT</b>	<b>3B</b>
Date:	Monday, February 16, 2009	Sheet 29 of 39



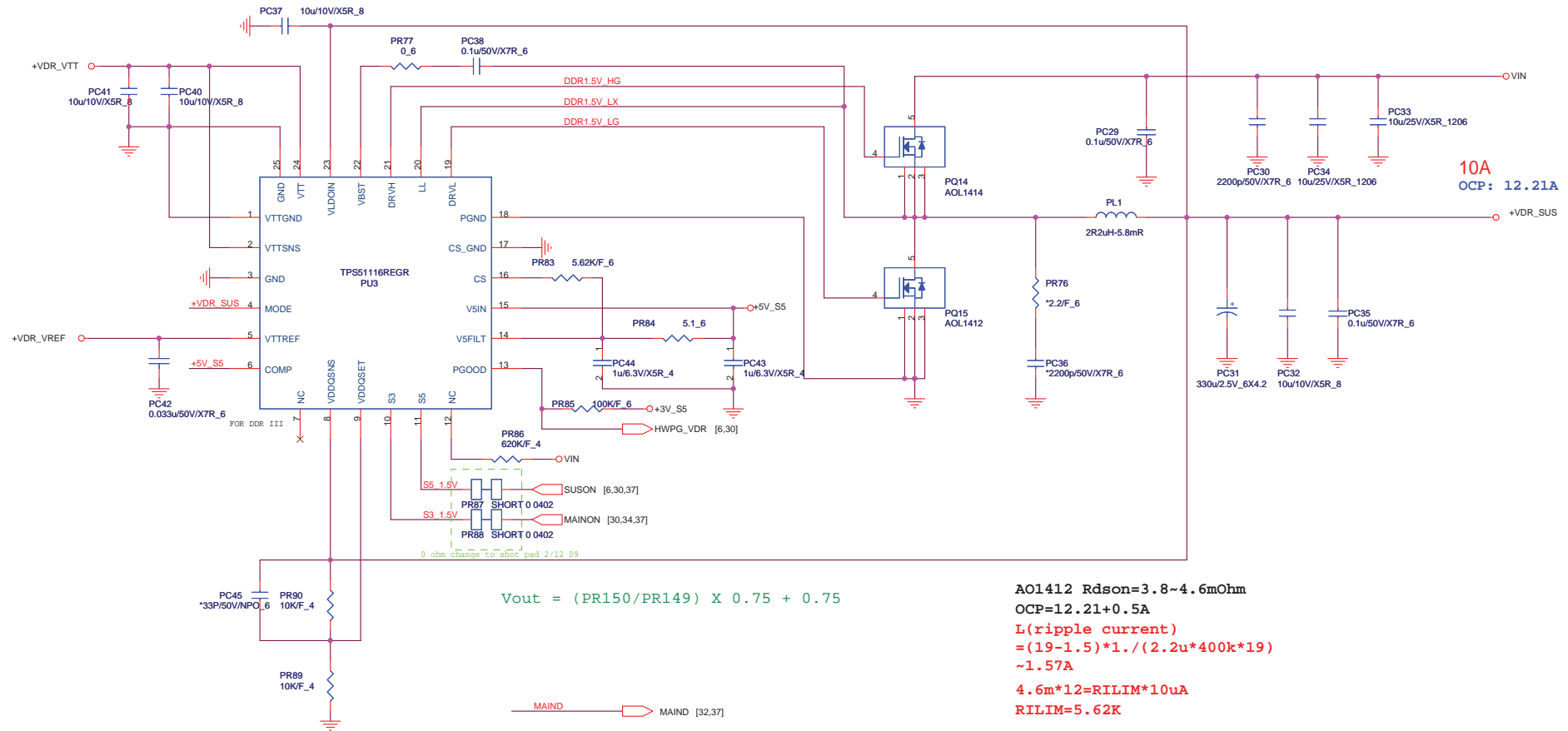












AO1412  $R_{ds(on)} = 3.8 \sim 4.6 \text{ m}\Omega$

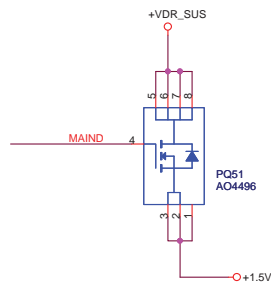
OCP = 12.21 + 0.5A

$L(\text{ripple current})$   
 $= (19 - 1.5) \times 1. / (2.2 \mu \times 400 \text{ k} \times 19)$   
 $\sim 1.57 \text{ A}$

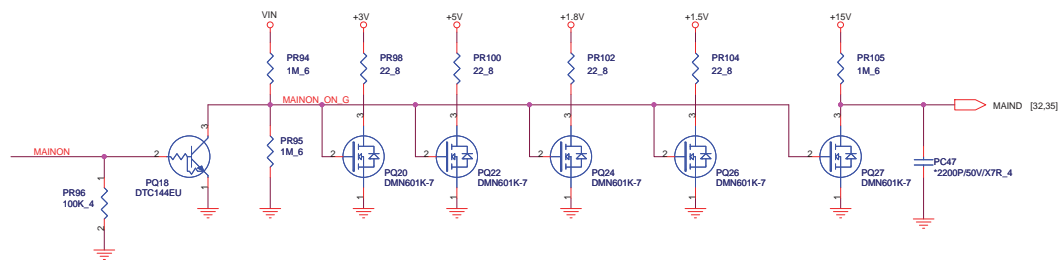
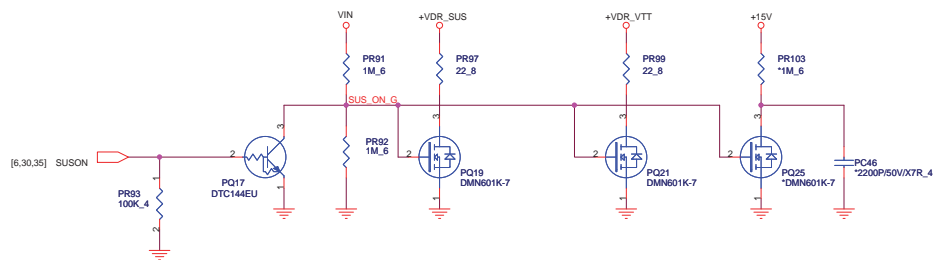
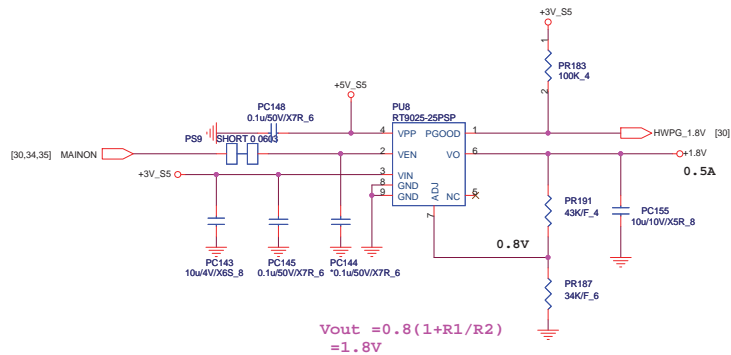
$4.6 \text{ m} \times 12 = \text{RILIM} \times 10 \mu \text{A}$

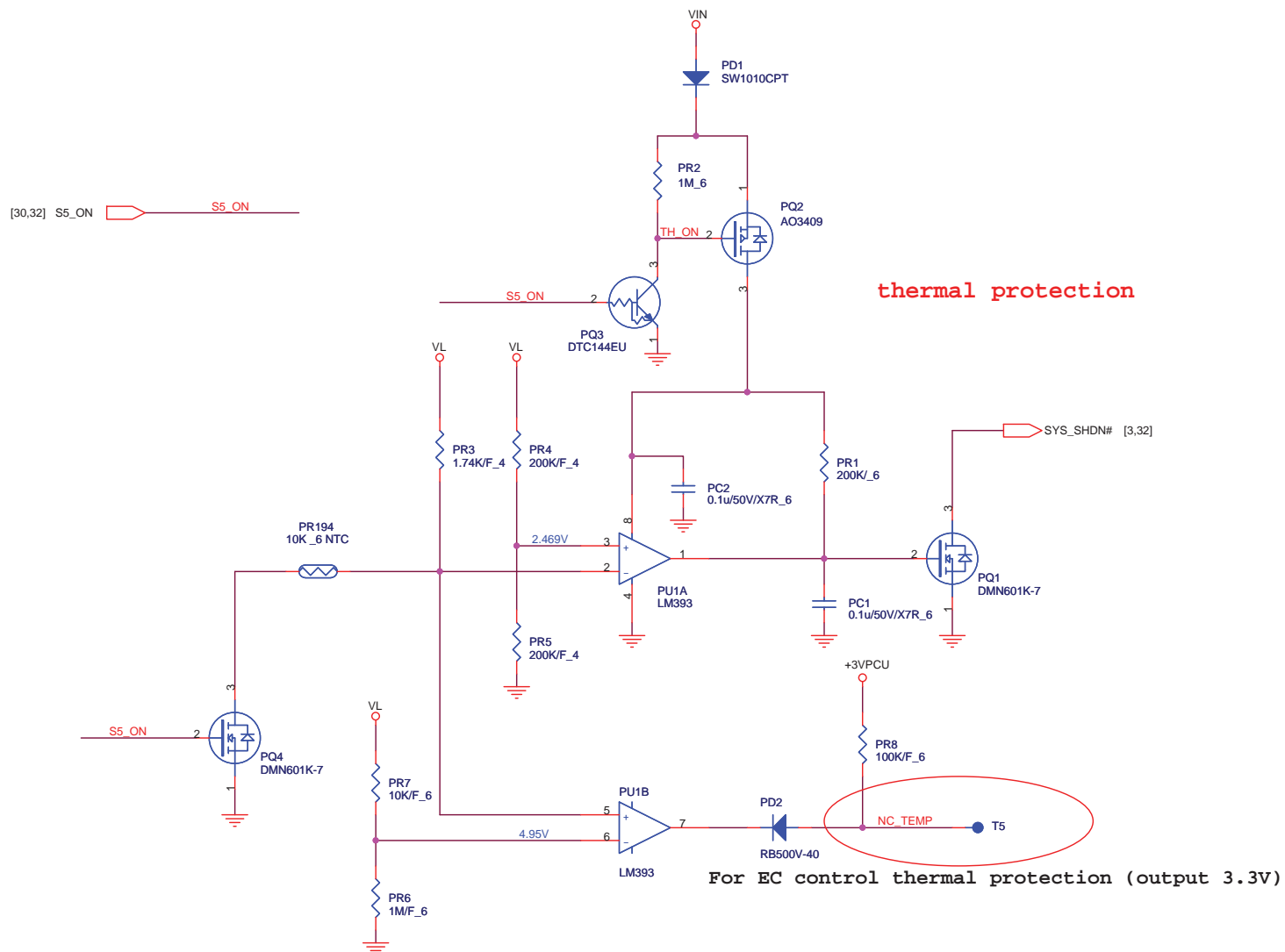
RILIM = 5.62K

$(10 \mu \times PR35) / R_{ds(on)} + \Delta I / 2 = I_{ocp}$









[illegible]